Technical Sessions
Mon., Sept. 28 – Wed., Sept. 30

Session 1 - Plenary Session
Monday Morning, September 28, Oak Ballroom

Session Chair: Kimo Tam, Analog Devices

8:00 am Welcome and Opening Remarks
Award Presentations
Keynote Speaker Introduction

Keynote Presentation
Dr. Fari Assaderaghi is Vice President of Advanced Technology Development at InvenSense.

Smart Low-Power MEMS Help Usher in the Wearable Era
Wearable devices are finally transitioning from hype to mainstream, aided by integration of valuable transducers, identification of application and use cases, ramp up of cloud services, and increased public awareness and interest due to Apple's watch introduction. Although still a nascent field, several themes are emerging:

- The wrist is only one of many targets for these devices. Smart glasses, hearables (ear as a natural place and rich with health information), necklaces, finger and hip worn products, and smart clothes are all becoming realities. Due to severe size constraints, several new user interfaces, such as audio, are becoming critical.

- Wearables are evolving from ability to perform simple functions such as step count, to becoming contextually aware products, providing richer user experience and data (health, fitness, infotainment, IoT control). These capabilities are in turn enabled by a plethora of transducers such as accelerometers, gyroscopes, magnetometers, pressure sensors, haptics, and microphones. Many new sensors and actuators are either being integrated or are just on the horizon: Heart Rate Monitor (HRM), Ambient Light Sensor (ALS), Ultraviolet detector (UV), temperature and humidity (RH&T) and gas and chemical sensors.

- Due to the desire for “always on” capability, small size limit, and appeal of charging only every few days, power is one of the most important parameters impacting the entire system design: Innovative circuit techniques target extreme low power. Smart combo sensors (MEMS SOC) handle tasks locally on chip instead of sending raw data to processor/cloud. Dedicated algorithms and software running on these smart combo sensors further reduce the system power (e.g. run-time calibration, streaming/batching of data, automatic activity recognition, heavy duty cycling of power-hungry functions such as GNSS). Finally, low-power wireless links enable connectivity of wearables to smart phones and other devices, and eventually to the cloud.

Session 2 - Low Power Analog
Monday Morning, September 28, Oak Ballroom

Session Chair: Shahrzad Naraghi, Tectronix
Session Co-Chair: Alessandro Piovaccari, Silicon Laboratories

This session focuses on low power analog circuits and techniques. Deep nanoscale CMOS designs, oscillators and a temperature sensor are highlighted.

10:00 am Introduction

10:05 am Scaling Analog Circuits into Deep Nanoscale CMOS: Obstacles and Ways to Overcome Them (INVITED), Peter Kinget, Columbia University, NY, NY

Analog circuits provide the critical interfaces between the digital world inside today’s integrated circuits and the physical world. Semiconductor technology scaling driven by ‘Moore’s Law’ has resulted in a phenomenal scaling of the performance of digital processors and memory. Continuing design innovations have enabled the scaling of analog interfaces onto scaled CMOS technologies, even though device scaling is a mixed blessing for the analog designer. This paper reviews the scaling challenges for analog circuits ranging from fundamental to practical challenges. Design strategies are outlined that in principle can overcome the challenges and can help guide the search for new circuit paradigms. Several examples of innovative analog design paradigms are reviewed and the opportunities in highly scaled CMOS technologies are outlined.

10:55 am A 51 pW Reference-Free Capacitive-Discharging Oscillator Architecture Operating at 2.8 Hz, H. Wang, P. P. Mercier, University of California, San Diego

This paper presents a gate-leakage-based Hz-range oscillator that achieves ultra-low-power frequency-stable operation in a small area via a capacitive-discharging architecture. Implemented in a 65 nm CMOS process, the proposed oscillator consumes 51 pW at 2.8 Hz and achieve a frequency variation of 937 ppm/oC from -40 °C to 60 °C.


2-2
2-3
This paper presents a novel ultra-low-power current-mode relaxation oscillator, which produces a 122kHz digital clock while dissipating 14.4nW at 0.6V. The self-biased frequency-compensated oscillator occupies 0.03mm² in 0.18µm CMOS and achieves a figure of merit of 120pW/kHz, making it one of the most efficient relaxation oscillators reported to date.

A 30.1µm², < ±1.1°C-3σ-Error, 0.4-to-1.0V Temperature Sensor based on Direct Threshold-Voltage Sensing for On-Chip Dense Thermal Monitoring, S. Kim, M. Seok, Columbia University

This paper presents an on-chip temperature sensor circuits that directly sense temperature dependency of threshold voltage. The sensor achieves a compact footprint of 30.1µm², error of <±1.1°C (3σ) across 0-100°C after one point calibration, and voltage scalability down to 0.4V without losing accuracy, making it suitable for on-chip dense thermal-monitoring.
In a classical PLL, the phase detector (PD) and charge pump (CP) noise is multiplied by $N^2$, where referred to the VCO output, due to the divide-by-N in the feedback path. It often dominates the in-band phase noise and limits the achievable PLL jitter-power Figure-Of-Merit (FOM). A sub-sampling PLL uses a PD that sub-samples the high frequency VCO output with the reference clock. The PD and CP noise in this PLL is shown to be not multiplied by $N^2$, and greatly attenuated by the high phase detection gain, leading to lower in-band phase noise and better PLL FOM. This article reviews the development of the PLL FOM, the sub-sampling PLL techniques and their applications in recent PLL architectures.

This paper presents a differential vector modulator phase rotator performing 360° full span phase interpolation over a first-ever decade-wide instantaneous bandwidth (2GHz-24GHz). A wideband poly-phase network based on folded transformer 90° couplers generates accurate differential quadrature signals with low passive loss (2dB) over a decade bandwidth. Two 5-bit linear digital variable gain amplifiers (VGAs) scale the quadrature signals, which are then combined for the target phase interpolations. Our phase rotator occupies a very compact chip size (1.2mm-by-1.8mm) in a standard 65nm CMOS process. Moreover, our design does not require any tuning element, band selection switch, or frequency-dependent code compensation/look-up table, ensuring that each phase interpolation code can be used for all the in-band operation frequencies. Additionally, the maximum RMS quantization phase error is only 1.22° within 1.5dB output magnitude variation for full 360° interpolation from 2GHz to 24GHz.

This paper presents a millimeter-wave fully differential compact transformer-based passive reflective-type phase shifter (RTPS). The proposed RTPS design employs two transformer-based 90° couplers and two transformer-based multi-resonance reflective loads, offering low-loss and an ultra-compact chip size. A proof-of-concept design at 62GHz is implemented in a standard 65nm CMOS process with a core area of 480μm-by-340μm. It achieves a wide phase shifting range (up to 367°) and a low insertion loss (IL) (3.7dB<|IL|<10.2dB) at 62GHz. It also performs phase shifting with a constant insertion loss at a loss variation of less than 0.7dB. Full-span 360° phase interpolation is achieved from 58GHz to 64GHz with a worst-case minimum IL of 10.72dB. Compared with the reported 60GHz RTPS integrated in silicon, our design is the first to achieve a full-span 360° phase shift, has the lowest IL and the smallest IL variation, and presents the best figure-of-merit (FoM) of 36.26°/dB.

This tutorial presents the design, analysis, and practical circuit implementation of low dropout regulators (LDOs). We begin with a review of traditional LDO regulator topologies and evaluate their key performance metrics such as dropout voltage, power supply rejection ratio, load and line regulation accuracy, settling time in the presence of load step, current efficiency, and stability. Following this, we describe alternate LDO architectures and illustrate how one can tradeoff some of the aforementioned performance metrics. We conclude with case study of a few state-of-the-art high performance LDOs.

Pavan Hanumolu is currently an Associate Professor in the Department of Electrical and Computer Engineering at the University of Illinois, Urbana-Champaign. He received the Ph.D. degree from the School of Electrical Engineering and Computer Science at Oregon State University, in 2006, where he subsequently served as a faculty member till 2013. Dr. Hanumolu’s research interests are in energy-efficient integrated circuit implementation of analog and digital signal processing, sensor interfaces, wireline communication systems, and power conversion.
Session 5 - Panel

Monday Afternoon, September 28, Oak Ballroom

1:30 pm Impedance Mismatch between Academia and Industry

Organizers:
Ayman Shabra, Masdar Institute of Science and Technology
Manoj Sachdev, Univ. of Waterloo

Panelists:
Elad Alon (Uni. Of California, Berkeley)
George Chien (MediaTek)
Peter Kinget (Colombia University)
Seyfi Bazarjani (Qualcomm)
Terri Fiez (Oregon State University)

This panel will explore to what extent should the training of graduate students enable their easy integration into today’s workforce. The very nature of long-term and predominately government sponsored research can create an impedance mismatch between industry and academia especially given the current stage of the lifecycle of the semiconductor industry. It will not be surprising if students learn fundamentals and skills that do not match the immediate needs of industry when they graduate. What is the extent of this mismatch and should we do something about it?

Session 6 - Analog Circuits Using Digital Cells

Monday Afternoon, September 28, Fir Ballroom

Session Chair: Jing Yang, Texas Instruments
Session Co-Chair: Arijit Raychowdhury, Georgia Institute of Technology

Analog circuits have been facilitated by digital cells. Technology of inverter based, ring oscillator based and standard digital cells are used to design the analog functions.

1:30 pm Introduction

1:35 pm 6-1 Design of PVT Tolerant Inverter Based Circuits for Low Supply Voltages (INVITED), Ramesh Harjani, Rakesh Kumar Palani, University of Minnesota

In this paper, we discuss traditional amplifiers and why inverter based amplifiers are better suited for lower supplies. We then describe the design procedure for inverter based OTA designs with an emphasis on PVT tolerant biasing. We finally validate our designs using measurement results.

2:25 pm 6-2 An 8bit, 2.6ps Two-Step TDC in 65nm CMOS Employing a Switched Ring-Oscillator Based Time Amplifier, B. Kim, H. Kim*, C. H. Kim*, Rambus Inc., *University of Minnesota

An 8bit two-step time-to-digital converter (TDC) with a novel digital switched ring-oscillator based time amplifier (TA) is demonstrated in 65nm CMOS. The proposed TA achieves a predictable and programmable gain without requiring any calibration. The implemented 8bit two-step TDC with a 16x TA gain achieves a time resolution of 2.6ps at 80MS/s conversion rate while consuming 2mW. The measured DNL and INL are 1.84LSB and 2.36LSB, respectively. The TDC area is 0.07mm².

2:50 pm 6-3 A Fully Synthesized 0.4V 77dB SFDR Reprogrammable SRMC Filter Using Digital Standard Cells, Jun Liu, Ahmed Fahmy, Taewook Kim, Nima Maghari, University of Florida

This paper presents a fully synthesized 0.4V analog Biquad filter in a 0.13µm technology using digital standard cells. A new fully reprogrammable multi-stage opamp array is introduced which can provide variable gain and bandwidth depending on the desired performance. In the proposed analog filter, all the active blocks such as the opamps and matched-RC duty-cycle generator are implemented using digital gates. This filter is implemented using Verilog code and synthesized using automated place and route. The prototype IC achieves 77.17dB peak SFDR and a tunable bandwidth of 1.7-2.5MHz while consuming 0.8mW power from a 0.4V analog supply and 1V supply for the switches.

3:15 pm Break
Monday Afternoon, September 28, Pine Ballroom

Session Chair: Christophe Antoine, Analog Devices
Session Co-Chair: Rikky Muller, Coretera Neurotechnologies

This session covers the latest advance in sensing, processing, power management and bidirectional telemetry for biomedical sensor systems.

1:30 pm  Introduction

1:35 pm  7-1

A 512x576 ISFET array is fabricated in CMOS 65nm process with high-gain (201mV/ph) readout by pH-to-voltage conversion and also with fast readout speed of 375 fps, towards DNA sequencing.

2:00 pm  7-2
A VoltageDoubling Passive Rectifier/Regulator Circuit for Biomedical Implants, Edward Lee, Alfred Mann Foundation

A circuit called prectulator is proposed in this paper. It utilizes the output transistor (MPR) of a linear regulator also as a passive rectifier for providing a regulated DC output from an AC input. The bulk voltage and the gate voltage (VG) of MPR are biased by an auxiliary rectifier and an error amplifier (AE), respectively. During startup and overload situations, overdriving MPR may occur and is prevented by limiting VG inside AE. Using this technique, a voltage doubling prectulator was implemented in a 0.18µm CMOS process. At 15MHz with a peak AC voltage of 3.6V, a power efficient of 87.7% and a voltage conversion ratio of 1.67 were achieved for a 6V output with a load power of 46.8mW.

2:25 pm  7-3

Reconstructing signals accurately is a critical aspect of compressed sensing. We propose a compressed-sensing sensor-on-chip that compresses and also extracts key statistics of the input signal at sampling time. These statistics can be used at the receiver to significantly improve the accuracy of reconstruction. When compared against a conventional compressed-sensing system, our experimental measured results demonstrate an improvement of as much as 9-18 dB in the signal-to-error (SER) of the reconstructed signal, depending on input data type and compression factor.

2:50 pm  7-4
A Full-Duplex Wireless Integrated Transceiver for Implant-to-Air Data Communications, S. Abdollah Mirbozorgi, Hadi Bahrami, Mohamad Sawan, Leslie Rusch, Benoit Gosselin, Laval University

A novel fully-integrated, full-duplex transceiver is presented. Unique features are: 1) RX and TX share the same antenna for minimum size, 2) dual band, RX uses a 2.4-GHz receiver for a 100-Mbps downlink, TX uses IR-UWB for a 500-Mbps uplink (10.8-pJ/b), and 3) size reduced by avoid using circulators/diplexers.

3:15 pm  Break

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Monday Afternoon, September 28, Silicon Valley Ballroom

Organizer: Dr. Mike Peng Li, Altera

This forum reviews the advancements in the past 1-2 years in silicon photonics and optical phase array ICs, as well as a forward looking discussion on quantum dot laser and silicon photonics. Key subjects covered includes: energy efficiency, modulation format, performance, density, testability, manufacturability, and reliability, and applications.

1:00 pm  Recent developments in Heterogeneously Integrated Photonics: Enabling the transformation of photonics from boutique to consumer-scale deployments, John Bowers (UCSB) and Alex Fang (Aurrion)

Impact of Quantum Dot Lasers on Silicon Photonics, Yasuhiko Arakawa (Tokyo University, Japan)

Monolithic Optical Phased Array Transceiver in Commercial Foundry CMOS SOI Process, Hossein Hashemi (USC)

Silicon Photonics in Mainstream Applications, Brian Welch (Luxtera)

Silicon Photonics Transformation from Technology of interest to Products, Bipin Dama (Cisco)
3:15 pm  Break

Educational Session 2

Monday Afternoon, September 28, Cedar Ballroom
Session Chair: Larry Nagel
Session Co-Chair: Larry Clark

1:30 pm  Behavioral Modeling Options For Balancing Verification Coverage and Credibility,  Jess Chen, Qualcomm

The purpose of verification is to reduce the risk of silicon not meeting performance specifications or worse yet, not functioning. Since the silicon does not yet exist, verification depends on simulations. Simulations in turn depend on models. In verification terms, the classical modeling tradeoff between speed and accuracy translates into a tradeoff between test coverage and model credibility (or validity). Transistor-level models produce the most credible simulations but slow run times and convergence problems severely limit test coverage. At the other extreme, a high level flat model quickly simulates all required tests but is least credible because the high level of abstraction greatly increases the chances for un-modeled circuit bugs and other relevant omitted behaviors. A “good” modeling boundary balances coverage and credibility. The balance is subjective because it depends on schedule, available resources, and acceptable risk. Given how strongly verification depends on the overall modeling strategy, it helps to have as many modeling options as possible. This tutorial describes a few modeling methods to balance coverage and credibility.

Jess Chen manages two groups of radio verification engineers at Qualcomm. Besides his relatively recent managerial duties, Jess has spent the last 20 years modeling RF systems and components at various companies. Before that, he spent 15 years at Lockheed Martin modeling and analyzing space craft power systems, motor drives, and unusual test equipment. Jess earned a BA in physics and applied math from UC Berkeley in 1977, an MSEE from San Jose State in 1982, the degree of engineer in control theory from Stanford University in 1985, and an MSME from Santa Clara University in 1991.

3:15 pm  Break

Session 9 - Advanced Simulation Techniques

Monday Afternoon, September 28, Oak Ballroom
Session Chair: Larry Nagel, Omega Enterprises Consulting
Session Co-Chair: Colin McAndrew, Freescale Semiconductor, Inc.

This session presents new methods for enhanced simulation techniques. The invited paper on this session describes the MAPP Platform from UC Berkeley.

3:30 pm  Introduction

3:35 pm  MAPP: The Berkeley Model and Algorithm Prototyping Platform (INVITED),  T. Wang, A. V. Karthik, B. Wu, J. Yao and J. Roychowdhury, University of California, Berkeley

We present the Berkeley Model and Algorithm Prototyping Platform (MAPP), a MATLAB-based framework for conveniently and quickly prototyping device compact models and simulation algorithms. MAPP's internal code structuring, which differs markedly from that of Berkeley SPICE and related simulators, allows users to add new devices with only minimal knowledge of simulation algorithms, and vice-versa. We describe MAPP's structuring and provide an overview of its capabilities. MAPP is available as open source under the GNU Public License.

4:25 pm  A System-Verilog Behavioral Model for PLLs for Pre-Silicon Validation and Top-Down Design Methodology,  A. Lotfy, S. Farooq, Q. Wang, S. Yaldiz, P. Mosalikanti, N. Kurd, Intel Corporation

A System-Verilog behavioral model for charge-pump PLLs based on piece-wise constant real number modeling and table lookup is presented. The proposed model exploits the sampled nature of the PLL where most of its analog behavior takes effect during phase detection. The model simulation run time takes only 1 second. Compared to transistor-level Spice simulations, the model shows a correlation of more than 97%. The PLL model is used to exercise critical features like spread-spectrum clocking and adaptive frequency system. In addition, the model was integrated in a pre-silicon validation environment and enabled catching design bugs.

4:50 pm  A Mixed-Domain Modeling Method For RF Systems,  Zhimiao Chen, Zhixing Liu, Lei Liao, Ralf Wunderlich, Stefan Heinen, RWTH Aachen
This paper introduces a mixed domain event driven modeling method for RF systems. The circuit behaviors are modeled in time/frequency domain adaptively combining with the equivalent baseband representation of each spectral component. Comparing to traditional baseband modeling methods or harmonic balance simulation techniques, this mixed domain method loose the requirements of relations among carrier frequencies of spectral components, and therefore can be widely used in mixed-signal circuit modeling. Furthermore, this method brings in a great simulation speed up over the simulation in passband signal abstraction, while the modeling accuracy can be guaranteed to meet the requirements of functional verifications.

### Session 10 - Memory Advancements

Monday Afternoon, September 28, Fir Ballroom

Session Chair: Dinesh Somasekhar, Intel
Session Co-Chair: Jean-Christophe Vial, Intel Mobile Communications

Advances in solutions for memory technologies ranging from DRAM, PCRAM, STTRAM, and SRAM are topics covered in this session.

3:30 pm **Introduction**

3:35 pm **10-1** Design Considerations of HBM Stacked DRAM and the Memory Architecture Extension (INVITED), Dong Uk Lee, Kang Seol Lee, Yongwoo Lee, Kyung Whan Kim, Jong Ho Kang, Jaejin Lee, Jun Hyun Chun, SK Hynix

Recently, the 3D stacked memory, which is known as HBM (high bandwidth memory), using TSV process has been developed. The stacked memory structure provides increased bandwidth, low power consumption, as well as small form factor. There are many design challenges, such as multi-channel operation, microbump test and TSV connection scan. Various design methodology make it possible to overcome the difficulties in the development of TSV technology. Vertical stacking enables more diverse memory architecture than the flat architecture. The next generation of HBM focuses on not only the bandwidth but also the system performance enhancement by adopting pseudo channel and 8-Hi stacking. The architecture applied to the second generation HBM are introduced in this paper.


Non-resistance read metric with drift resilient nature is enhanced to be suitable for high density memory array with large parasitic time constant. Experimental results for a bank of 2Gb multi-level density are demonstrated with total read latency of 450ns.

4:50 pm **10-3** A Fully-Functional 90nm 8Mb STT MRAM Demonstrator Featuring Trimmed, Reference Cell-Based Sensing, John DeBrosse, Thomas Maffitt, Yutaka Nakamura, Gorenelle Jan*, Po-Kang Wang*, IBM, *TDK

Spin Transfer Torque Magnetoresistive RAM (STT MRAM) has uniquely attractive write performance and endurance characteristics. Nonetheless, little STT MRAM circuit hardware data has been published. This paper describes a fully-functional 90nm 8Mb STT MRAM, identifies and describes solutions to the primary circuit challenges, and includes considerable circuit hardware data.


This paper presents 64-kb 8T three-port image memory using a 28-nm FD-SOI process technology. In the test chip, the energy minimum point is a supply voltage of 0.54V at a frequency of 18.2MHz, at which 298-fJ/write in a write operation and 650-fJ/cycle in a read operation are achieved.
This session showcases multiple state-of-the-art designs on wireless transceiver front-end as well as fully integrated power amplifiers including a dual-band linear digital polar power amplifier, a broadband mm-wave linear power amplifier and a mm-wave switching power amplifier.

3:30 pm  Introduction

3:35 pm  11-1  A Dual-Band 802.11abgn/ac Transceiver with Integrated PA and T/R Switch in a Digital Noise Controlled SoC (INVITED), Yuan-Hung Chung, Che-Hung Liao, Chun-Wei Lin, Yi-Shing Shih, Chin-Fu Li, Meng-Hsiung Hung, Ming-Chung Liu, Pi-An Wu, Jui-Lin Hsu, Ming-Yeh Hsu, Sheng-Hao Chen, Po-Yu Chang, Chih-Hao Chen, Yu-Hsien Chang, Jun-Yu Chen, Tao-Yao Chang, George Chien, MediaTech Inc.

This paper describes a dual-band 802.11abgn/ac compliant transceiver in a 4-in-1 combo connectivity SoC. It integrates the PAs, LNAs, T/R switches, and the 5GHz Balun. Due to the transmitter architecture and adaptive biasing scheme both are tailored for wide bandwidth, the 5GHz transmitter achieves 18.2dBm average output power for 802.11ac VHT80 MCS9 (Modulation and Coding Scheme 9). Within the 50MHz channel bandwidth, the IQ mismatch becomes frequency dependent, and is compensated through calibration. In the 2.4GHz transmitter, its PA load-line is adjustable. The power efficiency is thus remained similarly regardless the output power is at 20dBm for long range operation, or 8dBm for short range operation. By controlling the turn-on resistance of power island switch in digital baseband, and properly sizing the filler cap, the switching noise can be well controlled. The chip occupies 24.9mm² in 55nm 1P6M CMOS technology, where 1.3mm² is for 5GHz WLAN and 2.1mm² is for 2.4GHz WLAN/BT.


This paper presents a highly linear dual-band mixed-mode polar power amplifier in CMOS. An ultra-compact single-transformer passive network provides dual-band optimum load-pull impedance matching, parallel power combining, and double even-harmonic rejection. The mixed-mode architecture leverages both digital and analog techniques to suppress the AM-AM and AM-PM distortions.

4:50 pm  11-3  A 15 GHz-Bandwidth 20 dBm P_{sat} Power Amplifier with 22% PAE in 65 nm CMOS, J. Zhao, M. Bassi, A. Mazzanti, F. Svelto, University of Pavia

To generate high output power with high efficiency over large bandwidth, a design technique to embed classical coupled resonators networks into power splitters and combiners is presented for the first time. The realized PA shows 15 GHz bandwidth with 30 dB gain, 20 dBm output power and 22% PAE.

5:15 pm  11-4  A 28 GHz Inverse Class-F Power Amplifier with Coupled-Inductor based Harmonic Impedance Modulator, S. Y. Mortazavi, Kwang-Jin. Koh, Virginia Tech

This paper presents a 28 GHz class-F-1 power amplifier in 0.13-μm SiGe BiCMOS technology. The PA adopts a coupled-inductor based harmonic impedance modulator in order to terminate 2nd and 3rd harmonic load impedances appropriately for class-F-1 operation. The coupled coils essentially provide frequency-dependent inductance that is optimal to resonant out 2nd and 3rd harmonic reactive impedance. The PA achieve 40-42% PAE over 27.5 GHz to 29 GHz, peak 42% PAE at 28 GHz with 50 mW OP-1dB power, one of the highest PAEs ever reported in silicon-based PAs. At 6-dB backoff output power, the PAE is as high as 20%. Psat is 16.6 dBm.

Session 12 - Tutorial - Beyond CMOS: Large Area Electronics - Concepts and Prospects

Monday Afternoon, September 28, Cedar Ballroom

Session Chair: Robert Atiken, ARM
Session Co-Chair: Tetsuya Iizuka, Univ. of Tokyo

This embedded tutorial discusses recent advances in the field of large area electronics including organic and thin film transistors in addition to CMOS.

3:30 pm  Introduction

3:35 pm  12-1  Recent Development in High-Mobility Organic Field-Effect Transistors, Takaufumi Uemura, Osaka Univ.

4:25 pm  12-2  A hybrid Large-Area Electronics: A Solution for Low-Cost Mass-Parallel Operations, Reza Chaji, Ignis Innovations

5:15 pm  12-3  Build Your Own Chip: Plastic Ics via Printed Electronics, Lucian Shifren, ARM
Session 13 - Panel

Monday Afternoon, September 28, Silicon Valley Ballroom
3:30 pm  What is 5G?
Organizer(s): Stacy Ho (MediaTek)
Moderator name and affiliation: Ramesh Harjani (University of Minnesota)
Panelists: Chris Hull (Intel)
Steven Hong (Kumu Networks)
Payam Heydari (UC Irvine)
Sohrab Emami (Co-founder, SiBEAM)

The push to increase wireless data capacity up into the Gb/s realm is gaining speed and technologists around the world are racing to define what 5G will be. This panel features a few experts that will try to answer the question, “What is 5G?” Among the topics that will be discussed are mmWave, integration with WLAN, MIMO, and interference cancellation.

Poster Session

5:00 pm – 7:00 pm
Siskiyou/Cascade Ballroom

M-1  A Linear Transconductance Amplifier with Differential-Mode Bandwidth Extension and Common-Mode Compensation, Derui Kong, Sang Min Lee, Shahin Mehdizad Taleie, Michael Joseph McGowan, Dongwon Seo, Qualcomm Technologies, Inc
A transconductance amplifier with extended bandwidth, which is a critical block in various applications including amplifiers, filters and DACs is presented. The presented technique introduces a differential-mode negative capacitance while introduces the common-mode positive capacitance such that it extends the differential-mode bandwidth and compensates the common-mode stability. The proposed transconductance amplifier has been implemented for a DAC in CMOS 20nm to improve the distortion performance as a negative transconductance circuit, but the proposed technique is applicable to the wide range of circuits with a transconductor.

M-2  Low Power Analog Circuit Techniques in the 5th Generation Intel CoreTM Microprocessor (Broadwell), P. Mosalikanti, N. Kurd, C. Mozak, T. Oshita, Intel Corporation
Fabricated on a 14nm process technology node, the 5th generation CoreTM processors improve energy efficiency over the previous 22nm generation by up to 2.5x. Numerous optimizations in the analog circuits contributed - lower PLL Vmin, 150mV lower clock distribution Vmin, 3x DDR power reduction, 10x lower thermal sensor power and more.

M-3  A Compact, High Linearity 40GS/s Track-and-Hold Amplifier in 90nm SiGe Technology, D. Lal, M. Abbasi, D.S. Ricketts, North Carolina State University
We report a 40GS/s Track and Hold Amplifier in 90nm SiGe HBT technology with ENOB>4.9. Up to 19GHz input, SFDR3>68dB, THD3<-31dB and IIP3>44dBm are measured with 560mW consumed over 0.03mm² active die area. Linearity is better than existing SiGe and CMOS THAs at 40GS/s and 50GS/s and comparable to 50GS/s InP designs for less than half the power consumption.

M-4  A Seizure-detection IC Employing Machine Learning to Overcome Data-conversion and Analog-processing Non-idealities, Jintao Zhang, Liechao Huang, Zhuo Wang, and Naveen Verma, Princeton University
A seizure-detection system is presented wherein the analog frontend performs data conversion and feature extraction with greatly reduced accuracy requirements. A machine-learning algorithm enables retraining of a classification model to compensate feature errors, restoring performance from 443 to 4 false alarms (i.e., at the level of the baseline system).

M-5  A 550μm² CMOS Temperature Sensor Using Self-Discharging P-N Diode with +/-0.1°C (3σ) Calibrated and +/-0.5°C (3σ) Uncalibrated Inaccuracies, G. Chowdhury, A. Hassib*, Synaptics, *University of Texas at Austin
A 550μm² temperature sensor with a p-n diode in a first-order Δ-Σ loop is presented. It offers calibrated inaccuracy of ±0.1°C and uncalibrated inaccuracy of ±0.5°C over the measured 35°C-100°C range. This sensor is optimized to implement a distributed thermal monitoring system in large SoCs operating typically above 30°C.

M-6  A 16-channel, 1-Second Latency Patient-Specific Seizure Onset and Termination Detection Processor with Dual Detector Architecture and Digital Hysteresis, C. Zhang, M. Altaf, J. Yoo, Masdar Institute of Science and Technology
This paper presents an area-power-efficient 16-channel seizure onset and termination detection processor with patient-specific machine learning techniques. The proposed Dual-Detector Architecture (D2A) incorporates two area-efficient classifiers to achieve a high sensitivity and specificity of 95.7% and 98%, respectively. The overall energy efficiency is measured as 1.85μJ/Classification.
An Eight Channel Analog-FFT Based 450MS/s Hybrid Filter Bank ADC With Improved SNDR for Multi-Band Signals in 40nm CMOS, Hundo Shin, Rakesh Kumar Palani, Anindya Saha, Fang-Li Yuan*, Dejan Markovic*, Ramesh Harjani, University of Minnesota, “University of California Los Angeles

We present a complete implementation of a hybrid filter bank ADC based on an analog-FFT. The proposed structure enables the signal in each channel of the wide band system to be separately digitized using the full dynamic range of the ADC. The prototype is implemented in 40nm CMOS process.

A 14-bit 0.17mm² SAR ADC in 0.13μm CMOS for High Precision Nerve Recording, Anh Tuan Nguyen, Jian Xu, Zhi Yang, National University of Singapore

This paper presents a high-resolution, area- and power-efficient SAR ADC for high-precision nerve recording. It features a new “half-split” DAC array with integrated digital calibrations for automatic estimation and calibration of capacitor mismatches. As a result, the ADC precision can be substantially improved given the constraints on area and power.

A 0.04-mm² 0.9-mW 71-dB SNDR Distributed Modular ΔΣ ADC with VCO-based Integrator and Digital DAC Calibration, Y. Yoon, K. Lee, S. Hong, X. Tang, L. Chen, N. Sun, University of Texas at Austin

This paper presents a low-power and small-area VCO-based closed-loop ADC with two highlights. First, the ADC has a distributed modular architecture, which allows the ADC to be easily reconfigured for other resolution specifications. Second, a novel digital DAC mismatch calibration technique is proposed. It ensures high linearity in the presence of large DAC mismatches.

A 16nm Configurable Pass-Gate Bit-Cell Register File for Quantifying the Vmin Advantage of PFET versus NFET Pass-Gate Bit Cells, Jihoon Jeong, Francois Atallah, Hoan Nguyen, Josh Puckett, Keith Bowman, David Hansquine, Qualcomm Technologies, Inc

A 16nm configurable pass-gate bit-cell register file allows a direct comparison of NFET versus PFET pass-gate bit cells for early technology evaluation. The configurable pass gate enables either a transmission-gate (TG), an NFET pass gate, or a PFET pass gate. From silicon test-chip measurement, the register file with PFET pass-gate bit cells achieves a 33% minimum supply voltage (Vmin) reduction in a 16nm FinFET technology and a 40% Vmin reduction in an enhanced 16nm FinFET technology as compared to a register file with NFET pass-gate bit cells. Test-chip measurements highlight the superior benefits of the PFET drive current relative to the NFET drive current at low voltages. The Vmin improvement with a PFET pass-gate bit cell represents a paradigm-shift from traditional CMOS circuit-design practices.

Custom 6-R, 2- or 4-W Multi-Port Register Files in an ASIC SOC with a DVFS Window of 0.5 V, 130 MHz to 0.96 V, 3.2 GHz in a 28-nm HKMG CMOS Technology, Henry Hsieh, Sang H. Dhong, Cheng-Chung Lin, Ming-Zhang Kuo, Kuo-Feng Tseng, Ping-Lin Yang, Kevin Huang, Min-Jer Wang, and Wei Hwang*, TSMC, *National Chiao-Tung University

We describe custom 6R, 2/4W general-purpose register files (GRF) in an ASIC-based SOC, which has roughly a 2~3X smaller area, 2X faster speed, and 5X lower power than a logic-synthesized version. Hardware showed a DVFS window of 0.5 V @ circuit, 130 MHz to 0.96 V, 3.2 GHz.


A 14.8μVRMS integrated-noise (10Hz-100kHz) LDO using switched-RC sample-and-hold bandgap and current-mode chopped, any-load capacitor stable error amplifier in 0.25μm CMOS process is presented. It delivers maximum load of 100mA with dropout of 230mV and IQ of 40μA. It achieves PSR of 50dB at 10kHz for programmable output voltage of 1V-3.3V.

A Scalable and Reconfigurable 2.5D Integrated Multicore Processor on Silicon Interposer, Jie Lin, Shikai Zhu, Zhiyi Yu, Dongjun Xu*, Sai Manoj P.D.*, Hao Yu*, Fudan University, "Nanyang Technological University

This paper presents a 2.5D multicore processor, which is flexible to be organized into various multi-chip systems to meet different application requirements. The 2.5D I/O supports 12 way full-duplex communication each by a pair of 8Gbps SerDes, achieving a bandwidth of 24GB/s. The system consumes 1.08W in GF 65nm process.


The implementation of the SubBytes (or S-Box) step of the AES algorithm significantly contributes to the area, delay, and power of AES accelerators. Unlike typical logic gate S-Box implementations, we use full-custom 256x8-bit ROMs, which significantly improve performance and efficiency. We implemented a fully-unrolled, pipelined AES-128 encryption accelerator using ROM-based S-Boxes in 65nm bulk CMOS which operates at 2.2GHz and consumes 523mW at 1.0V, 27C. In counter-mode operation (CTR), the throughput is 275.2Gbps, which is 5.2x higher than the highest ever reported in the literature to our knowledge.

Efficiency Improvement Techniques for RF Power Amplifiers in Deep Submicron CMOS, Aritra Banerjee, Rahmi Hezar, Lei Ding, Texas Instruments

Integration of RF power amplifier in CMOS technology can help to reduce total solution cost and achieve small form factor in modern communication systems. This paper reviews recent developments in CMOS based PA architectures including PWM based digital transmitter and outphasing power amplifier and presents a multi-mode outphasing PA.
This paper presents the first wireless synchronization of a mm-wave array, eliminating the need for connecting wires between the array elements. Wireless injection locking is successfully demonstrated and a 3dB bandwidth of 400Hz at a carrier frequency of 50GHz is achieved (frequency stability of 8ppb). The chip includes two on-chip antennas, a power amplifier, a phase-shifter, buffer amplifiers, and a VCO. The chip is fabricated in a 65nm CMOS process and occupies an area of 1.7mm × 3.8mm.

A tunable oscillator based on phase interpolation has been studied. It utilizes delta sigma modulator to randomly select between the multi-phase outputs of a digitally-controlled injection-locked ring oscillator, thus achieving a low phase noise tunable high frequency reference that can be applied to normal integer-N PLL.

A 65nm 0.1-5.0GHz self-calibrated SDR transmitter is presented. A complete self-calibration scheme is proposed to alleviate the non-ideal effects, including RF operation frequency deviation, output power control, LO leakage and image suppression. A power mixer RF front-end and a V-I converter with 3rd-order nonlinearity cancellation are adopted to improve the CIM3 performance. A Class-AB/F dual-mode PA is integrated for narrowband applications.

A field-programmable noise-canceling wide-band receiver front end with high performance LNTAs is presented. The common-source (CS) and common-gate (CG) LNTAs are split into several cells whose bias point can be individually programmed in class AB and C yielding a highly linear hybrid class-AB-C LNTA. The 40nm LP CMOS receiver prototype can be programmed on the fly to adapt to different RF environments; it was tested in a low noise mode, a high linearity mode and a low power mode. Across these modes, the receiver has maximum gain of 53dB, a minimum NF of 2.2dB, a maximum B1dB of +11dBm, and a maximum OB-IIP3 of +21dBm; the signal path consumes between 15 and 40mA from a 2.5V supply and the LO current varies from 2.2 to 20mA from a 1.1V supply across operating frequencies. The measured LO emission at the antenna port is <-84dBm.

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Tuesday, September 29, 2015

Session 14 - Emerging Technology, Power and Cooling

Tuesday Morning, September 29, Oak Ballroom

Session Chair: Aurangzeb Khan, Altia Systems
Session Co-Chair: Arif Rahman, Altera Corporation

This session focuses on emerging technologies to enable future SoC applications including energy and power efficiency and leading edge integration.

9:00 am

Introduction

9:05 am


In modern integrated systems, interconnect and thermal management technologies have become two major limitations to system performance. In this paper we present a number of technologies to address these challenges. First, low-loss polymer-embedded vias are demonstrated in thick wafers compatible with microfluidics. Next, fluidic I/Os for delivery of fluid to microfluidic heat sinks are demonstrated in assembled 2.5D and 3D stacks. Next, thermal coupling between dice in 2.5D and 3D systems is explored. Lastly, the utility of microfluidic cooling is demonstrated through an FPGA, built in a 28nm process, with a monolithically integrated microfluidic heat sink.

9:55 am


An embedded microprocessor core designed to have high soft-error immunity via architectural, micro-architectural, and circuit techniques, is presented. Special automated place and route flows afford robustness against multiple node charge collection. The design is implemented on a commercial 90-nm bulk CMOS process. Silicon results, including error correction examples, are presented.

10:20 am

14-3 A 2.2 GS/s 188mW Spectrometer Processor in 65nm CMOS for supporting Low-Power THz Planetary Instruments, F. Hsiao, A. Tang, Y. Kim, B. Drouin*, G. Chattopadhyay*, M-F. Chang, UCLA, JPL

The paper presents a 2.2 GS/s (1.1 GHz Nyquist bandwidth), 188 mW 512-channel spectrometer processor developed to support future science observations on NASA planetary missions.
This paper presents the Arria 10 architecture, a high-density FPGA family using TSMC 20SOC, including an embedded ARM A9 subsystem, over 1M logic elements, 1.7M user flip-flops, 64Mb of embedded memory, 28G transceivers, hardened single-precision IEEE 754 floating point and PCIe sub-blocks, external memory controllers and advanced power management features.

This paper demonstrates an unconventional and fully automated approach to technology mapping for standard cell ASICS. It was used to fabricate a 32-bit signed 2-stage Wallace-Tree multiplier in a 65-nm LP technology, showing a significant reduction in power, leakage, area and wire-length, without sacrificing performance of the design.
time/area efficiency without an external microcontroller. In addition, the SSEOM determines the BER-optimal equalization parameters for both CTLE and DFE by incorporating a pattern-dependent eye-tracking scheme. Auxiliary data samplers are employed in parallel with data samplers to track link variations and adjust the equalization parameters in the background. A 28-Gb/s CDR including a SSEOM-based adaptive equalizer is fabricated in 40nm CMOS for an evaluation.

A 0.622-10Gb/s Inductorless Adaptive Linear Equalizer with Spectral Tracking for Data Rate Adaptation in 0.13-µm CMOS, S. Ray, M.M. Hella, Rensselaer Polytechnic Institute

This paper presents an inductorless adaptive equalizer with data rate adaptation based on dual-loop balancing technique and a third order nested feedback equalizing filter. Implemented in 130nm CMOS technology, the equalizer maintains an eye opening of 0.26, 0.44 and 0.5UI with BER<10^-12 for 5, 8.5 and 10Gb/s PRBS31 inputs, respectively.


In this paper, a ring oscillator based fractional-N DPLL that achieves low jitter by extending bandwidth using noise cancellation techniques is presented. A dual-path digital loop filter architecture is employed to resolve the ΔΣ DAC quantization noise challenge. Fabricated in 65nm CMOS process, the proposed PLL operates over a wide frequency range of 4GHz-5.5GHz and achieves 1.9psrms jitter while consuming only 4mW. The measured in-band phase noise is better than -96 dBc/Hz at 1MHz offset. The proposed FNDPLL achieves wide bandwidth up to 6MHz using a 50 MHz reference. The FoM is -228.5dB, which is at least 20dB better than all reported ring-based FNDPLLs.

Tuesday Morning, September 29, Pine Ballroom

Session Chair: Tanya Nigam, GLOBALFOUNDRIES
Session Co-Chair: Rajiv Joshi, IBM T. J. Watson Research Center

The first two talks in this session focus on the key challenges of further FINFETs scaling and optimization to enable SOC performance and power benefits. Final presentation reviews the time dependent variability in scaled technologies.

9:00 am Introduction


In this paper, we review the conditions at which FinFETs could meet system requirements at the 7nm node. We explore the key enabler to meet the power performance targets for 7nm node. We show that the device parasitics is the biggest performance detractor as we scale down. We illustrate the device design space that allows to meet speed and power targets, then explore the optimization of the geometry in combination with disruptive solutions such as air gap spacers and wrapped contacts, the benefits and drawbacks of increased fin height, and the design level solutions such as fin depopulation.

9:55 am Scaling Challenges of FinFET Technology at Advanced Nodes and Its Impact On SoC Design (INVITED), S. Banna, GLOBALFOUNDRIES

With the introduction of FinFET technology in mass production, more designs and complex designs are being ported on 22nm and 14nm/16nm FinFET transistors. However, all FinFET transistors are not made equal to offer best System-on-Chip (SoC) performance and power benefits. Careful selection of fin structural parameters is critical for best SoC performance. This paper discusses FinFET scaling challenges, their impact on SoC performance, key trade-offs and possible solutions for best SoC performance at current and future technology nodes.

10:45 am Break

11:00 am Characterization and Simulation Methodology For Time-Dependent Variability In Advanced Technologies (INVITED), P. Weckx1,2, B. Kaczer2, P. Raghavan2, J. Franco2, M. Simicic1,2, Ph. J. Rousset2, D. Linten2, A. Thean2, D. Verkest2, F. Catthoor1,2, G. Groeseneken1,2, 1 KU Leuven, Belgium, 2 Imec, Belgium

This paper describes the implications of Bias Temperature Instability (BTI) related time-dependent threshold voltage distributions on the performance and yield of devices and SRAM cells. We show that nFET and pFET time-dependent variability, in addition to the standard timezero variability, can be fully characterized and projected using a series of measurements on a large test element group (TEG) fabricated in an advanced technology. The statistical distributions encompassing both time-zero and timedependent variability and their correlations are discussed. The assumption of Normally distributed threshold voltages, imposed by State-of-the-Art design approaches, is shown to induce inaccuracy which is readily solved by adopting our defect-centric statistical approach.
Session 17 - Forum: Wireless Power for Biomedical Applications

Tuesday Morning, September 29, Silicon Valley Ballroom

Organizer: Ed Lee (Alfred Mann Foundation)

Wireless power delivery is widely used for powering implantable biomedical devices. In this forum, different fundamental issues in delivering power to the implants in the human body wirelessly will be addressed. State-of-the-art techniques for simultaneously delivering power to the implants and data communication with the implants will also be discussed.

9:00 am  
Coil-Based Systems for Neuroimplants: from Wireless Power and Data Transfer to Direct Neurostimulation, Gianluca Lazzi (University of Utah)

Wireless Power Delivery for Implantable Medical Devices, Wing-Hung Ki (Hong Kong University of Science and Technology)

Near Field Simultaneous Wireless Power and Data Transmission across the Skin, Maysam Ghovanloo (Georgia Tech)

Wireless power for tiny medical devices in the body, Ada Poon (Stanford University)

10:45 am  
Break

Educational Session 3

Tuesday Morning, September 29, Cedar Ballroom

Session Chair: Foster Dai, Auburn University
Session Co-Chair: Jay Wang, Intel

9:00 am  
Multiphase RF Techniques in CMOS Applied to Beam-forming and Full Duplex Receivers, Bram Nauta, University of Twente, The Netherlands

Modern CMOS technologies allow for multi phase RF circuits with interesting properties. Besides high Q filtering at RF (N-path filters) one can also easily manipulate the gain and phase of the RF signals during down-conversion. One application for this are compact implementations of multi-antenna beam-forming in phased-array receivers. Another application is self-interference cancelling in full duplex transceivers. In these latter transceivers transmission and reception occurs at the same time and at the same carrier frequency, requiring robust self-interference cancelling. In this Educational Session several examples of mutipath beam-forming and full duplex circuits will be explained.

Bram Nauta received his PhD in 1991 from the University of Twente, Enschede, The Netherlands. After 7 years in Philips Research labs, he returned as full professor, heading the IC Design group. He served as TPC member of the major conferences in the field, was program chair of ISSCC and the editor-in-chief of IEEE J. Solid State Circuits. Bram is IEEE Fellow, member of IEEE-SSCS AdCom and co-recipient of the 2002 and 2009 *ISSCC Van Vessem Outstanding Paper Award*.

10:30 am  
Break

Educational Session 4

Tuesday Morning, September 29, Cedar Ballroom

Session Chair: Howard Luong, Hong Kong University of Science & Tech.
Session Co-Chair: Foster Dai, Auburn University

11:00 am  
Phase-Locked Frequency Synthesis and Modulation for Modern Wireless Transceivers, Woogeun Rhee, Institute of Microelectronics, Tsinghua University, Beijing, China

Frequency synthesis and modulation by the DS fractional-N PLL are essential in modern wireless transceivers. In addition to loop parameter variability, leakage current, and matching problems, the DS fractional-N PLL needs to deal with quantization noise and nonlinearity in consideration of phase noise, spur, and settling time. In this talk, various fractional-N PLL architectures (analog/digital/hybrid) and recent circuit techniques for mitigating quantization and nonlinearity will be discussed. Also, PLL-based modulation methods (1-point/2-point/2*-point) will be overviewed.
Woogeun Rhee received the B.S. degree in electronics engineering from Seoul National University, Seoul, Korea, in 1991, the M.S. degree in electrical engineering from the University of California, Los Angeles, in 1993, and the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign, in 2001. From 1997 to 2001, he was with Conexant Systems, Newport Beach, CA, where he was a Principal Engineer and developed low-power, low-cost fractional-N synthesizers. From 2001 to 2006, he was with IBM Thomas J. Watson Research Center, Yorktown Heights, NY and worked on clocking area for high-speed I/O serial links, including low-jitter phase-locked loops, clock-and-data recovery circuits, and on-chip testability circuits. In August 2006, he joined the faculty as an Associate Professor at the Institute of Microelectronics, Tsinghua University, Beijing, China, and became a Full Professor in December 2011. His current research interests include clock/frequency generation systems for wireline and wireless communications and low-power transceiver systems for wireless body area networks. He currently holds 20 U.S. patents. Rhee served as an Associate Editor for IEEE Transactions on Circuits and Systems Part-II: Express Briefs (2008-2009) and a Guest Editor for IEEE Journal of Solid-State Circuits Special Issue in November 2012 and November 2013. He is currently an Associate Editor for IEEE Journal of Solid-state Circuits. He is also a member of the Technical Program Committee for several IEEE conferences including ISSCC, CICC, and A-SSCC.

Luncheon Keynote

Tuesday, 12:20 pm, September 29
Sierra Ballroom
Tickets for the luncheon are for sale at the Conference Registration Desk

The Technology Of Racing: Designing, Building And Racing Electric Motorcycles, Kenyon Kluge, Director of Electrical Engineering, Zero Motorcycles

Motorcycle racing is a sport that takes a balance of dedication, individual skill, team organization/effort, money, and technology. Racing electric motorcycles drastically increases the latter two (money and technology) in the equation and also adds the challenge of consumer and industry acceptance. Electric motorcycles and electric racing have made inroads into the motorcycle industry and consumer acceptance over the last 5 years but have also suffered from some setbacks that would have been difficult to predict at the outset. As a motorcycle racer for the last 18 years, and an electrical engineer for that same amount of time, I offer the perspective that the technology has advanced much faster than everyone had expected and where the setbacks are occurring are in the adoption of the technology and organization of promotional events like racing.

Session 18 - Data Converter Techniques

Tuesday Afternoon, September 29, Oak Ballroom
Session Chair: John McNeill, Worcester Polytechnic Institute
Session Co-Chair: Abhishek Bandyopadhyay, Analog Devices

This session presents six papers covering advanced data converter techniques across different architectures, including successive approximation, time-interleaved, folding, VCO-based, and non-uniform sampling ADCs.

2:00 pm Introduction

2:05 pm

18-1 ADC Trends and the SAR ADC Architecture (INVITED), Jeffrey Fredenburg and Michael P. Flynn, University of Michigan

2:55 pm

18-2 A Flash-Based Non-Uniform Sampling ADC Enabling Digital Anti-Aliasing Filter in 65nm CMOS, Tzu-Fan Wu, Cheng-Ru Ho, Mike Shuo-Wei Chen, University of Southern California

A different class of ADC architecture that non-uniformly samples the analog input but generates uniform digital output. The proposed ADC utilizes 4-bit voltage quantizer and time quantizer with 10 ps accuracy. Combined with the proposed digital anti-aliasing filter, it improves SNR by nearly 30 dB in comparison with a conventional 4-bit uniform sampling ADC.

3:20 pm


A two-step fully digital beat frequency quantizer based continuous time ADC is demonstrated in a 65nm test chip to achieve high resolution (6-7 ENOB) for direct conversion of low swing (<10mV) bio-potential signals. The resolution of ADC can be adaptively controlled depending on the input signal swing. A triple-sampling technique generates a synchronous ADC output from an asynchronous beat frequency quantizer. The proposed two-step ADC achieves a 44.5dB SNDR which is 5.6dB higher than the previously proposed single step architecture for a 10mVpp, 300Hz differential input signal.

3:45 pm Break
4:00 pm  
18-4  
Practical Considerations for Application Specific Time Interleaved ADCs, Aaron Buchwald, Hui Li, University of Texas at Dallas

4:50 pm  
18-5  
A 0.073-mm² 10-GS/s 6-bit Time-Domain Folding ADC in 65-nm CMOS with Inherent DEM, Shuang Zhu, Benwei Xu, Bo Wu, Kiran Soppimath, and Yun Chiu, University of Texas at Dallas

An area-efficient time-domain conversion technique is reported to achieve 10-GS/s, 6-bit resolution in 65-nm CMOS with area of 0.073 mm². The front-end single voltage-to-time converter (VTC) eliminates clock-skew calibration. The inherent folding effect helps significantly to lower the back-end complexity while built-in dynamic element matching (DEM) ensures good linearity.

5:15 pm  
18-6  
A 5Gs/s 10b 76mW Time-interleaved SAR ADC in 28nm CMOS, Fabian Silva-Rivas, Kwang Young Kim, Chaoming Zhang, Frank Singor, Broadcom Corporation

This paper presents a 5G's/s, 10b, 12X time-interleaved SAR ADC for multi-GHz direct sampling receiver applications. Many design techniques such as the top-plate sampling with merged capacitor switching, optimized circuit design of the sampling network, reference buffer, comparator and novel reference scheme enable this ADC to achieve one of the lowest FoMs. The digital calibration for offset, gain and timing skew in this TI-SAR ADC make it highly scalable to an advanced CMOS technology. As a result, this ADC achieves 49dB SNR, 52dB THD and 42dB SNDR in the Nyquist band while consuming 76mW from 1V supply and occupying 0.57mm² in 28nm CMOS technology.

Session 19 - Power Management

Tuesday Afternoon, September 29, Fir Ballroom

Session Chair: Hoi Lee, University of Texas at Dallas
Session Co-Chair: Jeff Morroni, Texas Instruments

Effective power management requires innovative techniques to minimize system costs while maximizing efficiency. This session covers a wide array of advances in power management spanning switched capacitor and high-frequency switching converters, LED drivers and wireless power.

2:00 pm  
Introduction

2:05 pm  
19-1  
Monolithic Very High Frequency GaN Switched-Mode Power Converters, Dragan Maksimovic, Yuanzhe Zhang, Miguel Rodriguez, University of Colorado

This paper describes very high frequency (10-200MHz) power converters using custom GaN chips with integrated power switches and gate drivers, allowing standard logic-level PWM control inputs, designed in depletion-mode 0.15μ RF and 0.25μm switch GaN-on-SiC processes. Operating from 25V, efficiencies exceeding 90% are demonstrated at up to 100MHz switching frequency.

2:30 pm  
19-2  
A 5 – 115V Efficiency-Enhanced Synchronous LED Driver with Adaptive Resonant Timing Control, Z. Liu, H. Lee, University of Texas at Dallas

A wide-input-range (5 – 115V) synchronous LED driver is presented in this paper. The proposed LED driver can automatically operate in the soft-switching mode to minimize the converter's switching loss in the HV condition. An adaptive resonate timing control (ARTC) is developed to generate optimal dead-time for establishing zero-voltage switching of both high- and low-side power FETs under different input and output voltages. Two high-speed HV body-diode-based zero-voltage detectors are also proposed to realize high-frequency soft switching. Implemented in a 0.5μm 120V CMOS process, the proposed LED driver can support up to 25 series-connected high-brightness LEDs. The LED driver can operate up to 1.6MHz and achieve a peak power efficiency of 94.4% in the soft-switching mode. Compared to the prior arts, the proposed LED driver is the first to demonstrate auto-configurable hard- and soft-switching capability by the ARTC to achieve high power efficiency and current accuracy over both widest ranges of the input voltage and the number of output LEDs.

2:55 pm  
19-3  
A 1A, 20MHz/100MHz Dual-Inductor 4-Output Buck Converter with Fully-Integrated Bond-Wire-Based Output Filters for Ripple Reduction, Y. Jiang, A. Fayez, Iowa State University

A Dual-Frequency Dual-Inductor Multiple-Output (DF-DIMO) buck converter in 65-nm CMOS with fully-integrated output capacitors is presented. The 2-phase input stage switches at 20 MHz and employs two 200-nH inductors, while the output stage switches at 100 MHz and generates four 250-mA outputs. Bond-wire-based filters are employed for voltage ripple reduction.

3:20 pm  
19-4  
Fast-Transient Asynchronous Digital LDO with Load Regulation Enhancement by Soft Multi-Step Switching and Adaptive Timing Techniques in 65-nm CMOS, Fan Yang, Philip K.T. Mok, The Hong Kong University of Science and Technology

The digital low-drop-out regulator (DLDO) load regulation enhancement technique including soft multi-step switching and adaptive timing for a finer-grained regulation is presented. Operating at 0.6V to 1V, a 65-nm asynchronous DLDO with this technique achieves a measured enhanced load regulation of 0.15mV/mA and nanoseconds’ 500mA
load transient response.

3:45 pm
Break

4:00 pm
3.5-0.5V Input, 1.0V Output Multi-Mode Power Transformer for a Supercapacitor Power Source with a Peak Efficiency of 70.4%. X. Hua, R. Harjani, University of Minnesota

A multi-mode 3.5-0.5V input, 1.0V output power transformer based on switched-capacitor DC-DC converters is designed to extract 98% of the energy from a 80mF supercapacitor. The circuit fabricated in TSMC’s 65nm process occupies an area of 0.48mm², supports a 3.3μA load current and operates at 2.0MHz, with a peak efficiency of 70.4%.

4:25 pm
A Near-Optimum 13.56 MHz Active Rectifier with Circuit-Delay Real-Time Calibrations for High-Current Biomedical Implants, C. Huang, T. Kawajiri, H. Ishikuro, Keio University

This paper presents a 13.56MHz active rectifier with enhanced power conversion efficiency (PCE) and voltage conversion ratio (VCR) for high-current biomedical implants. Near-optimum operation with circuit-delay compensation is achieved by the proposed real-time NMOS on/off calibrations, which minimize the reverse current and maximize the transistor conduction time under PVT variations.

4:50 pm
A Power Electronics Unit to Drive Piezoelectric Actuators for Flying Microrobots, Mario Lok, Xuan Zhang, Elizabeth Farrell Helbling, Robert Wood, David Brooks, Gu-Yeon Wei, Harvard University

This paper describes a power electronics unit (PEU) for an insect-scale flapping-wing robot. Three power saving techniques used in the actuator driver of the PEU-envelope tracking, dynamic common mode, and charge sharing-reduce power consumption while retaining weight benefits of an inductor-less linear driver.

5:15 pm
A 110nA Quiescent Current Buck Converter with Zero-power Supply Monitor and Near-constant Output Ripple, Danzhu Lu, Suyi Yao, Bin Shao, Analog Devices

A 110nA quiescent current buck converter is presented. A novel pull-down structure with native NMOS and PJEF is proposed to achieve zero-power supply monitor. Measured results show that the converter realizes 78% efficiency in 1μA load. With adaptive-bias hysteresis comparator, near-constant output ripple is achieved in full load range.

Session 20 - Manufacturing Beyond Moore's Law

Tuesday Afternoon, September 29, Pine Ballroom

Session Chair: Philippe Jansen, Texas Instruments Corporation
Session Co-Chair: Ramnath Venkatraman, Avago Technologies

The first paper discusses improvement in carrier mobility from alternative device materials combined with strain engineering techniques. The second paper describes how GaN power amplifiers get a 5x improvement over the incumbents GaAs and Si. The last two papers describe the benefits of 3D packaging and its application in 3D computing.

2:00 pm
Introduction

2:05 pm

This review focuses on material challenges associated with III-V co-integration with Si for future CMOS. There is a huge volume of literature on this topic as implementation of III-V monolithic integration with Si has been the holy grail for last four decades; targeting a wide range of applications including RF devices, LEDs, lasers, photo-detectors and the like. The key drivers have been the cost reduction, scalability with Si wafer diameter, and accessibility to highly scaled integrated circuits next to III-V devices. With the current focus on CMOS the pace of progress on monolithic integration has accelerated by leaps and bounds partly because of its vast impact on CMOS scaling, and partly due to the aggressive CMOS roadmap requirements. The discussion below concentrates on In0.53Ga0.47As channel which is the dominant III-V material being pursued for future technology. Despite the narrow focus, fundamental and engineering challenges posed by this material encompass a broad range of material topics including epitaxial growth, crystallographic defects and their dynamics during growth and subsequent processing, clever device architecture to alleviate adverse impact of defects on device leakage, and innovative engineering for material improvement.

2:55 pm
Recent Advances in GaN MMIC Technology (INVITED), N. Kolias, Raytheon Company

GaN MMIC technology is now in production and is revolutionizing microwave systems. In this paper we present an overview of GaN MMIC technology, focusing on device characteristics, reliability, and high frequency performance. We also introduce emerging GaN technologies such as GaN-on-diamond and the heterogeneous integration of GaN with Silicon.

3:20 pm
A Novel Low Cost, High Performance and Reliable Silicon Interposer (INVITED), Farhang Yazdani, BroadPak
Silicon interposer has emerged as a substrate of choice for integrating fine pitch, high density devices. Conventional packaging of 2.5D/3D devices involves multiple levels of assemblies. Normally, 2.5D/3D devices are first assembled on thinned silicon interposer with aspect ratio of 10:100 followed by second level assembly on a multi-layer organic build-up substrate. In this study we introduce direct assembly of silicon interposer on PCB, resulting in reduced cost and increased performance. We investigate effect of under-fill on solder joint reliability during direct assembly of silicon interposer on PCB. A 10x10mm^2 interposer test vehicle was designed and fabricated on 310um thick rigid silicon substrate. BGA of side of the interposer was bumped with eutectic solder balls through a reflow process. Interposer was then assembled on a 50x50mm^2 FR-4 PCB through a reflow process. We present cost analysis, design flow, and direct assembly of rigid silicon interposer on PCB. Effect of under-fill on the solder joint reliability is demonstrated using CSAM images during temperature cycles at 250, 500, 750 and 1000 intervals. It is shown that all samples successfully passed the temperature cycle stress test.

3:45 pm Break

4:00 pm Computing in 3D (INVITED), Paul Franzon, Eric Rotenberg, James Tuck, W. Rhet Davis, Huiyang Zhou, Joshua Schabel, Zhenquan Zhang, J. Brandon Dixel, Elliott Forbes, Joonmoo Huh, Steve Lipa, North Carolina State University

3D technologies offer significant potential to improve performance and performance per unit power. After exploiting TSV technologies for cost reduction and increasing memory bandwidth, the next frontier is to create more sophisticated solutions that promise further increases in performance/power beyond those attributable to memory interfaces alone. These include heterogeneous integration for trusted design and exploitation of the high amounts of interconnect available to provide for customization. Challenges include access for prototype quantities and the design of sophisticated static and dynamic thermal management methods and technologies.

Tuesday Afternoon, September 29, Silicon Valley Ballroom

2:00 pm Semiconductor Startups in the New Millennium

Organizers: Rikky Muller (Cortera Neurotechnologies)
Alireza Shirvani (Proteus Digital Health)

Moderator: Ali Niknejad (University of California, Berkeley)

Panelists:
Shahin Farshchi (Partner/VC, Lux Capital Management)
Michelle Kiang (Founder/CEO, Chip Microsystems)
Mike Noonen (Founder/Chairman, Silicon Catalyst; Interim CEO, Ambiq Micro)
Samuel Sheng (Founder/CEO, Sentons)
Mark Zdeblick (Founder/CTO, Proteus Digital Health)

Venture investment in semiconductor technology is near an all-time low. Yet – are there still opportunities for new companies? Definitely! Internet of Things and Healthcare technologies are just a couple of examples where semis can bring tremendous value and enable new disruptive technologies. Come hear about the opportunities and challenges from the entrepreneurs and investors themselves!

3:45 pm Break

Tuesday Afternoon, September 29, Cedar Ballroom

Educational Session 5

2:00 pm Supply noise induced jitter modeling and optimization for high-speed interfaces, Dan Oh, Altera

The supply noise impact plays a major role in designing modern high-performance SOCs or FPGA devices. A conventional power distribution network design to minimize supply noise can lead to significant oversizing and often times can no longer be implemented in a cost effective way. Optimal power distribution network can be designed based on modeling supply noise induced jitter and its impact on system-level performance, instead of focusing on noise reduction. This talk presents the key issues and challenges in high-speed link interfaces due to supply noise, the basics of supply noise induced jitter modeling, and unique design techniques for different signaling applications.
such as memory interfaces, serial links, and digital logic paths.

Dan Oh is a Signal and Power Integrity (Si/Pi) Architect at Altera where he is responsible for leading cross functional Si/Pi co-design teams including IC design, packaging, and product engineering as well as driving the overall Si/Pi technical direction. Dr. Oh was most recently a Technical Director at Rambus Inc. where he defined the signaling roadmap, supported system definition of new product proposals, and drove IP development for innovative signaling solutions. He has over 25 years of experience in the area of signal and power integrity. Dr. Oh received his Ph.D. in Electrical Engineering from the University of Illinois at Urbana-Champaign. He has numerous patents and papers in the areas of high-speed I/O modeling, simulation, and design. He is the lead author of the book High-speed Signaling: Jitter Modeling Analysis, and Budgeting, and also serves on the technical program committees of leading conferences such as IEEE EPEPS, IEEE ECTC, IEEE EMC SiPI, and IBM DesignCon.

3:30 pm Break

Tuesday Afternoon, September 29, Cedar Ballroom

Session Chair: Jay Wang, Intel
Session Co-Chair: Byunghoo Jung, Purdue University

4:00 pm MMIC for 5G, Ali Sadri -- Intel Corporation

Increasing the capacity of next-generation backhaul and access networks is becoming one of the most challenging tasks of the industry this decade. As traditional mechanisms to increase spectral efficiency approach their theoretical limits, new and disruptive techniques are needed to satisfy the growing demand of mobile data traffic. Consequently, the fifth generation (5G) cellular access system is expected to make extensive use of small cells to increase the density and capacity by several hundred times in comparison with 4G systems. Not only cellular access, wireless backhaul solutions require increased density and capacity. While considerable focus has been rightfully put into exploiting licensed frequency bands below 6 GHz, the vast amount of licensed frequency spectrum in millimetre wave (mmWave) bands has seen little use by cellular access systems despite holding far greater potential for enhancing capacity. Not only licensed spectrum, unlicensed mmWave spectrums (57-63GHz) can be considered for wireless backhaul solutions. This presentation introduces novel architectures, beamforming, RFIC and manufacturing for mmWave capable small cells (MCSCs) with modular antenna arrays for backhaul and access. This architecture makes use of heterogeneous network components combined with the use of mmWave based technologies for the backhaul, fronthaul and access. We show that MCSCs can significantly increase capacity and density for backhaul and access systems.

Dr. Ali Sadri is Sr. Director of mmWave Standards and Advanced Technologies at Intel Corporation. His Professional work started at IBM, who was responsible for communications standards, in year 1990 and a Visiting Professor at the Duke University through year 2000. During years 2000-2002 he joined BOPS Inc., a startup company specialized in programmable DSP’s as the Sr. Director of the Communications and Advanced Development. In 2002 Ali joined Intel Corporation’s Mobile Wireless Division where he initiated and lead the standardization of the next generation High Throughput WLAN at Intel that became the IEEE 802.11n standards. Later Ali founded and led the Wireless Gigabit Alliance since 2008 that created the ground breaking WiGig 60 GHz technology. In June 2013 WiGig Alliance merged with WiFi Alliance to advance and certify the WiGig programs within WiFi alliance framework. Currently Ali is leading the mmWave advanced technology development that includes the next generation WiGig standards and mmWave technology for 5G cellular systems for future backhaul and access networks. Ali holds more than 100 Issued and pending patent applications in wired and wireless communications systems.

Siskiyou/Cascade Ballroom

5:00 pm – 7:00 pm

T-1 A Novel Switched-Capacitor-Filter Based Low-Area and Fast-Locking PLL, M. Amourah, M. Whately, Cypress Semiconductor

A new low-area and fast-locking Phase Locked Loop (PLL) is presented. The proposed PLL employs a new switched capacitor (SC) filter that uses fractional charge integration to implement capacitor multiplication effect. The proposed (SC) filter has a time response similar to the traditional passive filter response while occupying much smaller area. The proposed PLL was built in a 65nm CMOS process with a capacitance multiplication factor of 16 in parallel with a traditional filter for performance comparison. The PLL has an operating frequency range of 200MHz to 2.0GHz. The PLL has period jitter in the order of 0.9ps RMS with acquisition time less than 10µS. Traditional LPF area is 180µm x 340µm while the (SC) LPF area is only 104µm x 84µm cutting LPF area by a factor 7

T-2 A Low TC, Supply Independent and Process Compensated Current Reference, Chundong Wu, Wang Ling Goh, Chiang Liang Kok, Wanlan Yang and Liter Siek, Nanyang Technological University, Singapore
This paper presents a 10-μA, trim-free, low temperature coefficient, supply independent current reference with process compensation feature. Based on the proposed structure, a 130 ppm/°C temperature coefficient current reference across -40°C to 80°C temperature range is achieved.

T-3 A 72µW, 2.4GHz, 11.7% Tuning Range, 212dBc/Hz FoM LC-VCO in 65nm CMOS. Joo-Myoung Kim, Jae-Seung Lee*, Suna Kim*, Taeik Kim, Hojin Park, and Sang-Gue Lee*, Samsung Electronics, *KAIST

An ultra-low power and wide tuning range LC-VCO is presented, where the performances are improved by identifying and avoiding the Q-factor degradation factors in the LC-tank. By the positioning analysis and adoption of MIM capacitor arrays along with minimum size varactors, the proposed VCO with a high-Q inductor, implemented in a 65-nm CMOS technology, operates from 2.35GHz to 2.64GHz (11.7% tuning) with phase noise of -132.92 dBc/Hz at 1MHz offset while dissipating only 72µW from a 0.6-V supply. The FoM of the proposed VCO is 212dBc/Hz and the widest tuning range is shown in the high-Q oscillators.

T-4 All-digital SoC Thermal Sensor using On-chip High Order Temperature Curvature Correction, Mehdi Saligane, Mahmood Khayatzadeh*, Yiqun Zhang, Seokhyeon Jeong, David Blaauw, Dennis Sylvester, University of Michigan, *Oracle

Accurate, compact thermal sensors are desirable in many applications, including on-chip temperature monitoring for processors with dynamic throttling and reliability management. Current sensors are limited in either area, robustness, or accuracy. This work sidesteps strong linearity requirements for reference and PTAT elements in the sensor by performing a higher-order fitting of more relaxed PTAT and CTAT elements using an embedded calculation compute engine. A compact 24 × 10µm sensing element (40nm CMOS) achieves inaccuracy of <1°C across 30 chips with 2-point calibration and a resolution of 0.02°C.

T-5 A Configurable 5.9 µW Analog Front-End for Biosignal Acquisition, Tan Yang, Junjie Lu*, M. Shahriar Jahan, Kelly Griffin, Jeremy Langford, Jeremy Holleman, University of Tennessee, *Broadcom Corporation

This paper presents a configurable analog front-end (AFE) for the recordings of a variety of biopotential signals. The AFE has a mid-band gain from 45.2-71 dB. The low-pass corner is tunable in the range of 70-400 Hz and 1.2-7 kHz. The AFE achieves high noise-power efficiency.

T-6 Ultra-Low Power Multi-Channel Data Conversion with a Single SAR ADC for Mobile Sensing Applications, Wenjuan Guo, Youngchun Kim, Ahmed Tewfik, and Nan Sun, The University of Texas at Austin

Based on the recently emerging compressive sensing theory, the paper proposes an ultra-low power multi-channel data conversion system whose architecture is almost as simple as a single SAR ADC. The proposed architecture is capable of simultaneously converting multi-channel sparse signals while running at the Nyquist rate of only one channel.

T-7 A 10.5-b ENOB 645nW 100kS/s SAR ADC with Statistical Estimation Based Noise Reduction, Long Chen, Xiyuan Tang, Arindam Sanyal, Yeonam Yoon, Jie Cong*, and Nan Sun, University of Texas at Austin, George Washington University

This paper presents a power-efficient SNR enhancement technique for SAR ADCs. By accurately estimating the conversion residue, it can suppress both comparator noise and quantization error. Thus, it allows the use of a noisy low-power comparator and a relatively low resolution DAC to achieve high resolution. The proposed technique has low hardware complexity, requiring no change to the standard ADC operation except for repeating the LSB comparisons. A prototype ADC is designed in 65nm CMOS. Its SNR is improved by 7dB with the proposed technique. Overall, it achieves 10.5-b ENOB while operating at 100kS/s and consuming 645nW from a 0.7V power supply.

T-8 A 12b ENOB, 2.5MHz-BW, 4.8mW VCO-Based 0-1 MASH ADC with Direct Digital Background Nonlinearity Calibration. K. Ragab, N. Sun, The University of Texas at Austin

A direct digital background calibration technique to correct nonlinearity errors in VCO-based 0-1 MASH SD ADCs is presented. The proposed technique altogether corrects VCO gain error, nonlinearity, and capacitor mismatch of the residue generating DAC. It improves SNDR of the prototype ADC from 60dB to 73.4dB in 2.5MHz signal bandwidth. The ADC consumes 4.8mW from 1.8V supply in 180nm CMOS. The measured convergence time is only 64ms.

T-9 A 130nm Canary SRAM for SRAM Dynamic Write $V_{MIN}$ Tracking across Voltage, Frequency, and Temperature Variations, A. Banerjee, J. Breitholz, B. H. Calhoun, University of Virginia

This paper shows the first silicon results of a working 512b canary SRAM using bitline and wordline type reverse assists in a 130nm bulk technology. The 512b canary SRAM has distinct canary failure trends across voltage, frequency, and temperature variations to track an 8Kb SRAM’s dynamic write $V_{MIN}$.

T-10 A Low Energy SRAM-based Physically Unclonable Function Primitive in 28 nm CMOS. A. Neale, M. Sachdev, University of Waterloo

A 0.6V low energy 64-kb SRAM-based PUF protected with a multi-bit ECC is fabricated in a 28nm LP-CMOS process. Majority voting and data integrity masking is used to reduce the parity-bit overhead by 65% to yield 100% reproducible PUF responses. Measurement results show an average active access energy of 0.045fJ/bit-cycle.

T-11 A 0.4V–1V 0.2aWm2 70% Efficient 500MHz Fully Integrated Digitally Controlled 3-Level Buck Voltage Regulator with On-Die High Density MIM Capacitor in 22nm Tri-Gate CMOS, Pavan Kumar, Vaibhav A. Vaidya, Harish Krishnamurthy, Stephen Kim, George E. Matthew, Sheldon Weng, Bharani Thiruvengadam, Wayne Proefrock, Krishnan Ravichandran, Vivek De, Intel Corporation

Circuit techniques to reduce inductor size are attractive to increase power density for On-Die Voltage Regulators. This paper
A Single-Inductor 7+7 Ratio Reconfigurable Resonant Switched-Capacitor DC-DC Converter with 0.1-to-1.5V Output Voltage Range, Loai G. Salem, Patrick P. Mercier, University of California San Diego

This paper demonstrates the first 7-ratio resonant switched capacitor (SC) converter using only a single inductor, in CMOS. A frequency-scaled-gear-train recursive topology is introduced that enables soft-charging of all flying-capacitors through one inductor at any arbitrary binary ratio. The converter achieves 14.4% efficiency improvement over co-fabricated SC in 0.18µm bulk.

A 83fps 1080P Resolution 354 mW Silicon Implementation for Computing the Improved Robust Feature in Affine Space, Shouyi Yin, Peng Ouyang, Leibo Liu, Shaojun Wei, Tsinghua University

In comparison with the popular feature algorithms in vision applications, AFFINE-SIFT (ASIFT) achieves the highest robustness in terms of illumination, rotation, and scale in affine space but exhibits high computation complexity. This work proposes three optimization techniques, including reverse based pipelined affine computing, full parallel Gaussian pyramid computing and rotation invariant binary pattern (RIBP) based feature vector computing, to accelerate the computation intensive parts in ASIFT, and design a high efficient pipelined and parallel architecture for the whole ASIFT. Using TSMC 65 nm process, silicon implementation shows that this work achieves the processing speed of 83fps@1080p (1000 feature points per frame on average) with 200 MHz while dissipating 354 mW. It fully supports the real time processing of high resolution images in vision scenes with strong robustness.


A wide tuning range 60GHz DCO with fine frequency step is presented. Different tuning techniques are combined to achieve 24% tuning range with a fine frequency resolution of 39 kHz. The phase noise at 1 MHz is -95.1dBc/Hz. The FOM of DCO is -186.4dBc/Hz which is better than recent DCOs.

A Cartesian Feedback-Feedforward Transmitter IC in 130nm CMOS, Sungmin Ock, Hyejeong Song, Ranjit Gharpurey, The University of Texas at Austin

A transmitter architecture based on Cartesian feedback-feedforward is described. A Cartesian feedback loop is used to linearize a transmitter and PA, and the error signal is utilized in a feedforward path to further enhance linearity. A proof-of-concept prototype transmitter IC that is used to linearize an external PA is demonstrated in a 130nm CMOS process. The implementation allows for a 8.7 dB ACLR improvement, compared to an open-loop transmitter, for an output power of 16.6 dBm at 2.4 GHz while employing a 16 QAM LTE signal with 1.4 MHz bandwidth.

A 0.6-V, 30-GHz Six-Phase VCO with Superharmonic Coupling in 32-nm SOI CMOS Technology, Dongseok Shin, Sanjay Raman, Kwang-Jin Koh, Virginia Tech

This paper presents a six-phase VCO using a superharmonic coupling technique. Three VCOs are coupled by an inductive network in their tail nodes to generate six-phase outputs. This network also serves as a tail noise filter in each VCO. Therefore, the proposed six-phase VCO can achieve better phase noise performance than typical multiphase topologies. The proposed VCO is implemented in 32nm SOI CMOS process with core area of 0.6×0.5mm2. The VCO can be tuned from 29.24 GHz to 31.56 GHz, a frequency tuning range of 7.6% at 0.6V supply. With each VCO consuming 1.52 mW DC power (4.56 mW total), the 60GHz VCO achieves -97 and -143 dBc/Hz PN at 30kHz and 3MHz offset, respectively.


A dual tank hard-clipping VCO is presented that can approach the maximum thermodynamically achievable oscillator FoM within 3dB. Compared to class-B/C/D/F oscillators, it is capable of reducing both close-in and far-out phase noise (PN). A prototype 4.17-to-4.95GHz VCO achieves -97 and -143 dBc/Hz PN at 30kHz and 3MHz offset, respectively.

A DC-to-12.5Gb/s 4.88mW/Gb/s All-rate CDR with a single LC VCO in 90nm CMOS, J. Yoon, S. Kwon, H. Bae, KAIST

The proposed CDR supports reference-less all-rate operation with static fractional divider and asynchronous phase calibration scheme. And the IC features an automatic loop gain control scheme which adjusts the bandwidth of a CDR automatically in the background for optimum BER performance. The power efficiency of the test chip is 4.88mW/Gb/s.

A High-Performance, Yet Simple to Design, Digital-Friendly Type I PLL, A. Sharkia, S. Aniruddhan*, S. Shekhar, S. Mirabbsai, University of British Columbia, *Indian Institute of Technology Madras

A 2.2-to-2.8 GHz 6.8 mW Type-I PLL occupies 0.12 mm² in 0.13-μm CMOS and achieves 490 fs rms random jitter, -103.4 dBc/Hz in-band phase noise, -65 dBc reference spur, and 2.5 μs lock-time. Lock range is improved using a saturated-PFD, voltage booster and a digital level shifter, and reference spur is suppressed using a S/H envelope detector.

Wednesday, September 30
This session will present analog techniques applied at high frequencies. For tunable filters, a PLL and track-and-hold amplifier.

9:00 am Introduction

9:05 am 22-1 A 4.6mW, 22dBm IIP3 all MOSCAP Based 34-314MHz Tunable Continuous Time Filter in 65nm, Rakesh Kumar Palani, Ramesh Harjani, University of Minnesota

An inverter based filter design is proposed that uses only MOSCAPs as filter capacitors. A 3rd order 34-314 MHz tunable continuous time filter is fabricated in TSMC's 65nm technology. The filter achieves an OIP3 of +25.24 dBm while drawing 4.2mA from a 1.1V supply and occupies an area of 0.007 mm².

9:30 am 22-2 2-4 GHz Q-Tunable LC Bandpass Filter with 172-dBxHz Peak Dynamic Range, Resilient to +15-dBm Out-of-Band Blocker, Laya Mohammadi, Kwang-Jin Koh, Virginia Tech

This paper presents a new Q-enhancement LC bandpass filter capable of 2.25~4.5 GHz frequency tuning range with independent Q control from 3 to 150. A dual varactor inverse (DVI) control method is proposed to suppress varactor nonlinearity. Also, the BPF employs a dynamic negative resistance circuit that introduces a gain peaking when the filter output reaches 1-dB gain compression point, extending the P-1dB input power. The circuit is implemented in a 0.13 μm SiGe BiCMOS process. Measurement results show 9~8 dBm of maximum IP-1dB, 10~18.5 dB of minimum NF, resulting in 147-172 dBxHz of normalized dynamic range when Q varies from 3 to 150. The BPF consumes 13-20 mA from 3.3 V supply. Chip size is 0.63×0.63 mm².

9:55 am 22-3 An Injection Locked PLL for Power Supply Variation Robustness Using Negative Phase Shift Phenomenon of Injection Locked Frequency Divider, Donggil Lee, Taeho Lee, Yong-Hun Kim, Young-Ju Kim, Lee-Sup Kim, KAIST

This paper presents a 2 GHz injection-locked PLL (ILPLL) with an injection-locked frequency divider(ILFD). Using a negative phase shift phenomenon of the ILFD, injection timing can be calibrated without a delay line. As a result, the proposed ILPLL achieves a simple background injection timing calibration for robustness of power supply variation. The test core has been fabricated in 65nm CMOS process consuming 3.74mW at 0.9V supply voltage.

10:20 am 22-4 A 200-MS/s 98-dB SNR Track-and-Hold in 0.25-μm GaN HEMT, S. Chung*, H.-S. Lee, Massachusetts Institute of Technology, *University of Southern California

In order to overcome the design challenges of GaN HEMT leakage and Schottky diode turn-on, a GaN track-and-hold (T/H) circuit with 20-V pseudo-differential input swing consists of an asymmetric gate device followed by a symmetric gate device. The GaN T/H provides 98-dB SNR at 200 MS/s while drawing 195 mA.

10:45 am Break

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This session presents compact models for emerging “More-than-Moore” devices as well as modeling and statistical techniques accounting for device variability.

9:00 am Introduction

9:05 am 23-1 Physics-based Compact Models for Insulated-Gate Field-Effect Biosensors, Landau-Transistors, and Thin-Film Solar Cells (INVITED), M. A. Alam, P. Dak, M. A. Wahab, X. Sun, Purdue University, West Lafayette

As the future of Moore’s law appear uncertain, semiconductor electronics is being reinvented with a broader focus on energy efficient 3D computing, flexible electronics, biosensors, energy harvesting, etc. These devices are gradually being integrated onto the CMOS fabric as ‘More-than-Moore’ components, with transformative impact on consumer electronics. Unfortunately, a lack of physics-based, experimentally validated, numerically stable, well-documented compact models makes integration of these components in a CMOS design flow difficult. In this paper, we describe physics-based compact models for three very different components that are likely to be integrated in future systems, namely, FET-based nanobiosensors for pH sensing, Landau-transistors for low-power electronics, and thin-film solar cells for energy harvesting. Our physics-based approach should inspire the community to develop similar models for...
other emerging devices, so as to make their integration onto CMOS platform a routine affair.


The development of a scalable and user-friendly SPICE model is a key aspect of exploring the potential of spin-transfer torque MRAM (STT-MRAM). A self-contained magnetic tunnel junction (MTJ) SPICE model is proposed in this work which can reproduce realistic MTJ characteristics based on user-defined input parameters such as the free layer's length, width, and thickness. Using the propose model, scalability studies of both in-plane and perpendicular MTJs can be performed across different technology nodes with minimal effort, which differentiates this model from most previously reported models.

10:20 am Symmetry Breaking in the Drain Current of Multi-Finger Transistors, N. Lu, S. Lee, R. A. Wachnik, IBM

The drain current of a multi-finger MOSFET is typically calculated as the product of that of a single-finger MOSFET and the number of fingers. Careful investigation of currents in different fingers of a multi-finger transistor in the presence of parasitic effects shows differences between the per-finger drain current of the multi-finger transistor and the drain current of a corresponding single-finger transistor. We show that each of the following factors alone causes the drain current in one or more fingers of a multi-finger transistor to be different from that in other fingers of the transistor and the per-finger drain current of the multi-finger transistor to be different from the drain current of a corresponding single-finger transistor: (a) the resistance of wires that connect multiple fingers together, (b) the contact resistance, (c) the diffusion resistance, and (d) self heating. Excluding all of the above factors, the uncorrelated variations among the sub-threshold drain currents of different finger cause the per-finger median sub-threshold drain current of the multi-finger transistor to be different from the median sub-threshold drain current of the single-finger transistor.

10:45 am Break

11:00 am Fast Statistical Analysis of Rare Circuit Failure Events via Bayesian Scaled-Sigma Sampling for High-Dimensional Variation Space, S. Sun, X. Li, Carnegie Mellon University

In this paper, we propose a novel Bayesian scaled-sigma sampling (BSSS) technique to analyze the rare failure events of nanoscale ICs in a high-dimensional space. An SRAM sense amplifier example designed in a 45 nm CMOS process is used to demonstrate the efficacy of BSSS.

**Session 24 - 5G mm-Wave and Next Generation Wireless Systems**

Wednesday Morning, September 30, Pine Ballroom

Session Chair: Julian Tham, Broadcom
Session Co-Chair: Wooguen Rhee, Tsinghua University

This session covers techniques for next generation wireless systems. The first paper describes design issues for 5G mm-wave systems. In the second paper, a dynamic waveform shaping technique with pico-second time resolution is demonstrated for sensing, imaging, and spectroscopy applications. The last paper presents wireless power and data transmission for implantable medical devices.

9:00 am Introduction

9:05 am A Circuit Designer’s Guide to 5G mm-Wave (INVITED), Ali M. Niknejad, Berkeley Wireless Research Center (BWRC), Siva Thyagarajan, Qualcomm Corporation, Elad Alon, Berkeley Wireless Research Center (BWRC), Yanjie Wang, Intel Corporation, Christopher Hull, Intel Corporation

The fourth generation mobile phone standards (4G) in widespread use include Long Term Evolution (LTE) and LTE-A (Advanced), which support up to 44 bands internationally, or an aggregate bandwidth of about 1 GHz in TDD and FDD modes. Techniques such as carrier aggregation allow the mobile operator to maximize bandwidth and deliver high data rate to users. As demand for wireless connectivity continues to grow exponentially, a fifth generation (5G) standard is envisioned, with the requirement to deliver higher throughputs, more spectrum—particularly in the mm-wave bands—higher capacity through spatial diversity, and lower latency. The projected deployment date of 5G is in 2019, and various proposals are under consideration. This paper will highlight important implications for the design of transceivers for 5G, particularly those targeting the mm-wave bands.


The paper presents a scalable architecture which can generate and radiate reconfigurable periodic waveforms with picosecond time-widths by quasi-optically interfering multiple delayed signals with rich harmonics. The chip is demonstrated to radiate pulse trains of 2.6ps time-widths, pure tones at 107.5GHz, 215GHz and any combination of these two harmonic frequencies.

10:20 am Advanced Wireless Power and Data Transmission Techniques for Implantable Medical Devices (INVITED), H.-M. Lee, M.Kiani**, M. Ghovanloo**, Massachusetts Institute of Technology, *Pennsylvania State University, **Georgia
Institute of Technology

This paper reviews various mechanisms for wireless power transmission with focus on efficient link structures and circuit techniques for implantable medical devices. These devices also require wireless data telemetry for wideband bidirectional data communication in the presence of the strong power carrier interference. This paper discusses several modulation schemes and transceiver circuits for low-power, carrier-less, and robust wireless data transmission.

10:45 am Break

Session 25 - 20 Gb/s Transmitters and Receivers

Wednesday Morning, September 30, Oak Ballroom

Session Chair: Jun Cao, Broadcom
Session Co-Chair: Shahriar Mirabbasi, University of British Columbia

This session presents innovative techniques for low-power 20 Gb/s optical and electrical transmitters and receivers.

11:00 am Introduction

11:05 am 25-1
A 20 Gb/s 0.3 pJ/b Singe-Ended Die-to-Die Transceiver in 28 nm-SOI CMOS, B. Dehlaghi, A. C. Carusone, University of Toronto

A low-power transceiver architecture for die-to-die applications is presented. The proposed transceiver employs CMOS logic-style circuits and a passive equalizer in the transmitter to reduce the power consumption. Single-ended signaling without a shared reference voltage is used to minimize the number of required signal traces and packaging bumps. A transceiver prototype is fabricated in 28 nm STM FD-SOI CMOS technology and it operates at 20 Gb/s and 16.4 Gb/s data rates over different channels with 5.9 and 7.1 dB of loss relative to DC (10.7 and 12.9 dB total loss) at the Nyquist frequency while consuming 0.30 and 0.33 pJ/bit excluding clocking circuits, respectively.

11:25 am 25-2
A 4×20-Gb/s 0.86pJ/b/lane 2-Tap-FFE Source-Series-Terminated Transmitter with Far-End Crosstalk Cancellation and Divider-less Clock Generation in 65nm CMOS, Shuai Yuan, Liji Wu, Ziqiang Wang, Xuqiang Zheng, Wen Jia*, Chun Zhang, Zhihua Wang, Tsinghua University, *Research Institute of Tsinghua University in Shenzhen

A 4×20Gb/s SST transmitter with 2-tap FFE and FEXT cancellation is presented. The FFE and XTC are merged together with the SST driver. The proposed divider-less clock generation saves much power. Fabricated in 65nm CMOS, the transmitter achieves a maximum data rate of 20Gb/s with a power efficiency of 0.86pJ/b/lane.

11:50 am 25-3
A 20Gb/s 0.77pJ/b VCSEL Transmitter with Nonlinear Equalization in 32nm SOI CMOS, Mayank Raj, Manuel Monge, Azita Emami, California Institute of Technology

This paper describes an ultra-low-power VCSEL transmitter in 32nm SOI CMOS. To increase its power efficiency, the VCSEL is driven at a low bias current. The resulting nonlinearity and loss in bandwidth is modelled and compensated by a nonlinear equalization technique that achieves 0.77pJ/b power efficiency at 20Gb/s.

Educational Session 7

Wednesday Morning, September 30, Cedar Ballroom

Session Chair: John McNeill, Worcester Polytechnic Institute
Session Co-Chair: Mohammad Ranjbar, Inphi Corporation

9:00 am SAR ADCs in time-interleaved converter arrays, Ron Kapusta, Analog Devices

The time-interleaved ADC was first published more than 30 years ago, yet recently has experienced a surge in interest, as the demand for increased bandwidth has outstripped the performance capability of existing single-core ADCs. Concurrent with this trend has been recent focus on the SAR ADC architecture. As it turns out, the SAR ADC is particularly well-suited for use in time-interleaved arrays. This tutorial talk will review the use of highly-parallel and time-interleaved converter arrays, including both the benefits provided to and the additional constraints placed upon the system. Similarly, the SAR architecture will be examined, demonstrating how its trade-offs, as compared to other ADC architectures, interact almost synergistically with the time-interleaved configuration. Finally, a number of case studies will be presented to highlight some recent advances in achieving very high data throughput while maintaining the required accuracy. Enabling design and calibration techniques will be covered.

Ron Kapusta received the B. S. and M. Eng. degrees from the Massachusetts Institute of Technology, in 2001. Upon
graduation, he joined Analog Devices, designing data converters and sensor interface circuits for multiple channel data acquisition systems. More recently, he has been with the Automotive Technology group, working on signal acquisition for MEMS-based inertial systems. Ron has presented at multiple IEEE conferences in addition to journal papers. He holds more than 40 U.S. and international patents and won the 2013 JSSC Best Paper award. He has served on the technical program committees for CICC and VLSI Circuits.

10:30 am Break

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**Session 26 - Forum- Advanced Power Amplifier Techniques for Mobile Devices**

Wednesday Afternoon, September 30, Oak Ballroom

**Organizers:**
Yanjie Wang (Intel)
Debopriyo Chowdhury (Broadcom)

The focus of this forum is on how to exploiting impedance transformation techniques in integrated CMOS Power Amplifiers for average power efficiency boosting. Impedance modulation is a powerful technique that can help boost efficiency at lower average power levels for power amplifier and can even be extended to wideband signals. We are going to explore suitable and efficient methods of achieving impedance transformation in CMOS integrated power amplifiers - which can enhance average efficiency, thereby improving overall battery life in portable applications.

**1:30 pm**

- **A Dual Mode Transformer-Coupled CMOS Class AB Power Amplifier with Back-Off Efficiency Enhancement**, Debopriyo Chowdhury (Broadcom Corporation)
- **Leveraging RF Power DACs to Enhance the Doherty Power Amplifier and Broadband Power Amplifier**, Hua Wang (Georgia Tech)
- **mm-Wave Digital Power Amplifier with Dynamic Load Modulation**, Eric Kerherve (University of Bordeaux)
- **Power Efficient PA matching design on Advanced CMOS Technology**, Hongtao Xu (Fudan University, Shanghai, China)
- **Switched Capacitor RFDACs For Power Efficient Multimode Transmitter**, Michael Fulde (Intel)

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**Educational Session 8**

Wednesday Afternoon, September 30, Cedar Ballroom

**Session Chair:** Jay Wang
**Session Co-Chair:** Byunghoo Jung

**1:30 pm**

**Resonant Wireless Power Transfer: Technology and Integration Roadmap**, Francesco Carobolante, Qualcomm

The promise of Resonant Wireless Power Transfer to enable seamless user experience while charging a variety of mobile devices with differing power requirements (from wearable and mobile devices to tablets and notebooks) is finally reaching maturity. While the specifications are now available and hardware is shown to be capable of charging devices from less than 1W up to 50W, the process of integration is now on the way, in order to address coexistence of the technology with the rest of the system, as well as size and cost constraints. After an introduction to Magnetic Resonance Wireless Power Transfer technology, this presentation will provide an overview of the challenges and trade-offs that led to the development of its specifications (including frequency selection, efficiency and thermal requirements, and other regulatory and use case considerations). Circuit implementations for both Transmitter and Receiver will be introduced, with a focus on new silicon and packaging technologies that enable high levels of integration, especially in space-constrained wearable devices and high power applications like notebooks.

Francesco Carobolante is Vice President of Engineering at Qualcomm Incorporated. In this position, he has been responsible for the development of products and technologies for mixed signal Integrated Circuits (primarily in Power Management and analog subsystems). He is currently leading the development of Wireless Power Transfer technology and its standardization through A4WP (the Alliance for Wireless Power). Prior to joining Qualcomm, he held positions at STMicroelectronics, Tripath Technology and Fairchild Semiconductors, developing analog, power, and MEMS based mixed signal products. He holds more than 50 patents and has published several papers on power, mixed signal and system design. He received an Electrical Engineering and PE degrees from the University of Padova in Italy, and a MSEE from UCLA.