BACK END VLSI DESIGN AND CHALLENGES: A PERSPECTIVE FOR EE ECOSYSTEM DEVELOPMENT

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1. What is Structural Design?
2. Logic and physical optimization process
3. Signoff flows in SD
4. Structural Design team skillset
5. What Defines DFM process?
6. LV process from DFM perspective: challenges
7. LV skillset
What is Structural Design?
In the context of civil engineering...

“The objective in structural design is to produce a structure capable of resisting all applied loads, according to design specifications, without failure during its intended life.”
What is Structural Design?

At Intel...

What happens in between?

- Circuit optimization cycle
- Sign-off checks.

Structural design engineers!
Structural Design process

Floor planning, logic synthesis, placement, clock tree synthesis, routing and ECO.
Floorplanning:
Divide and conquer approach for SoC design

Design hierarchy:

Floorplanning:
The only way to manage a design of hundreds of millions of transistors is to break it up into smaller blocks.

- Functionality aware partitioning.

Design challenges: area, aspect ratio, power and clock distribution.
Floorplan design:
Fully abutted floorplan style

Floorplan engineers:
• Determine sub designs area and shapes.
• Aligned pin placement.

SD execution engineers:
• Each sub design has a dedicated team of experts working on it.
  • EDA tools run on each sub.
  • A full chip team integrates the complete design with the SoC.
Some considerations:

- Areas with higher frequency logic need a denser grid to deliver more current.
- Gated power is used for some areas of design to turn on/off certain logic blocks.

**Design challenges:** power dissipation and physical phenomena effects.

Primary goal: transfer RTL description of the fub into a gate level netlist.

Design challenges: trade off between power, timing and area.
Placement optimization
Smart component positioning

Placement: process of determining the locations of components on a die surface.

- Legalization: process of arrange cells in legal positions.

**Design challenges:** timing performance, routability, heat distribution, power consumption.
Clock Tree Synthesis
Real clocks implementation

Up to this point, design has been using virtual clocks.

The purpose of CTS is to deliver clock signals to sequential elements by making interconnections from the clock generators in the chip to all subunits.

Global clock distribution
Clock network design for correct synchronization

Equal distribution of clock signal to all flip-flops and latches to avoid skew.

Routing Optimization
Global and detailed routing

Routing defines precise paths for conductors that carry electrical signals to interconnect all pins electrically equivalent.

Design challenges: wire length, timing constraints, manufacturing design rules (resistance, capacitance, metal layer spacing, wire/via width, etc.)

**Placed design**

**Global routing**

**Detailed routing**


Engineering Change Orders (ECO)

Types of ECOs:
- Change in functional logic (gate-level netlist ECO)
- Compensation of design errors.

Pros:
- Save time: avoid going through complete synthesis flow.
- Save money: especially after mask design is done.

Design challenge: formal equivalence checking.
Sign-off verification flows in Structural Design
Timing Verification (TV)
Static timing analysis (STA)

Timing is a major consideration in the synthesis and physical implementation of synchronous digital circuits.

Static timing analysis (STA) is a method of validating the timing performance by checking all paths under **worst-case** conditions.

Two major factors in STA:
1. Cell delays
2. Interconnect delays and layout parasitics

Timing path.

Detailed RC parasitics.
Timing Verification (TV)

Signal integrity

Signal Integrity analysis allows to identify noise effects on circuit functionality due to crosstalk, distortion and loss caused by electromagnetic coupling.

Formal Verification (FV)

Formal Verification proves the functional equivalence between two different representations of the same design.

Main steps:
- Translate both designs to a mathematical format in Boolean domain
- Establish correspondence between the two designs
- Prove equivalence or non-equivalence.

\[ R_1 \equiv r_1 \]
\[ X \equiv X \]
\[ Y \equiv Y \]
\[ R_2 \equiv r_2 \]
Reliability Verification (RV)
IR drop, electromigration, self-heating and more

RV covers several **physical phenomena and electrical overstress conditions** which may lead to immediate failure or gradual deterioration of a chip performance or functionality.

The aim of RV is to guarantee reliability (in performance and functionality) over the entire product life cycle.

Reliability verification checks **Electromigration (EM), Self Heat (SH)** and **IR drop**.
Structural Design engineering teams skillset

- **SD execution owners**
  - Organization
  - Debug & Analysis
  - Teamwork

- **Signoff checks**
  - Debug and analysis
  - Self-driven
  - Programming and scripting
  - Problem solving

- **Technical Managers**
  - Teamwork
  - Technical leadership
  - Communication skills and networking
Layout Verification Team (LV): focus area

• Key role to provide DFM tape in quality completion for given projects.
• DFM process is defined by technology, client and schedule aspects.
• Logic/analog circuit, base and metal fill challenges.
• LV is a multidisciplinary team that handles many aspects of DFM convergence.
• Roles and responsibilities, brief description.
What defines Design for Manufacturability process (DFM)?

**Technology requirements:**

- Intel researches new processes and incoming technologies.
- Defines tendency for next years (Moore’s law), cloud computing, internet-of-things, wearable tech.
- New tech products face many design and factory challenges, unexpected scenarios and new rules, based on real time experiences.
Customer specifications:

✓ Major server, desktop, mobile and phone manufactures uses Intel-based systems.

✓ Design methodologies must be developed to meet either client needs on time as well technology requirements.

✓ Product cannot go to fab with DFM issues.
Schedule:

✓ Product impacts market and company revenue.

✓ Based on certain windows (CES, back-to-school, Christmas).

✓ Product needs to bring all technical specifications at planned delivery time.
LV Process: defined from DFM perspective

Interaction of logical nets with surrounding components

Design for manufacturability

Meet density rules for metal / via layers

Chip meets yield expectative and technology quality

Meets ground/power stability and density rules for diffusion and device-related layers
Design challenge:
convert a circuit design into a high volume product

Facts:

- Meet DRC rules (end to end and gap separation) using signal nodes only is not possible with latest technologies.
- Router cannot drop detailed results, runtime and rule complexity forces to match some partial checks.
- Timing values are calculated (realistic, pessimistic), but until post silicon analysis all these data becomes real (critical for tech lead vehicle projects).
- Vendor software is used for design and analysis (customized by enclose internal requirements), but complex issues needs in-house solutions.
Metal fill challenges for DFM: be aware of new RC aggressor

- Active and dummy fill will perform final DR completion, affecting directly RC, noise and circuit timing.
Metal fill challenges for DFM: **transition areas**

Same layer width not used along the chip.

Cleanup to zero violations results complex, especially over transition areas.
Base fill challenges: many layers at same level

Base layer represent a high amount of layers place in same level.

Connectivity, design rules and density must match technology requirements

The 32nm planar transistor (on left) illustrates current (represented by yellow dots) flowing in a flat plane under the gate, while Intel’s smaller 22nm 3-D Tri-Gate transistor (on right) illustrates increased current flow over three sides of a vertical fin.

Content from http://www.intel.com, called How Intel Makes Chips: Transistors to Transformations
Engineering work: functions within LV team

LV is a multidisciplinary team that handles many aspects of DFM convergence.

Electronic engineers, VLSI expert, computer science engineers and project managers are part of the team.
LV: team positions and responsibilities.

- Analog and digital focus.
- Layout implementation.
- ECO application.
- Final DR cleanup.
- Last mile conversion.

- Methodology definition.
- Project technical support.
- Section/Chip integration.

- Physical Design Engineer
- Computer Science Engineer
- Process / Project owner
- Manager

- Vendor-2-Intel tool sync.
- Custom SW solutions.
- Process automation.
- New technology research.
- Team management.
- People development.
- Resources and assignments.
- Portfolio (long term strategy).
Physical Design Engineer (PDE).

Two specializations for this job title: **analog and digital circuits**.

Layout implementation:
- Debugs layout verification flows and complex design problems.

ECO application:
- Many detailed schematic changes can be done by synthesis, but incremental fixes can be done only by PDEs.

Final DR cleanup (Last mile conversion):
- Get layout verifications ready for tape in, passing all design rules.
- Ensure all necessary collateralas are generated for final chip level runs.
PDE qualifications

• Layout debug.

• Understanding of process specifics (design rules, power constrains) as well technology characteristics (min and max density rules, new layer interactions, via rules, standard cells methodology, IP-block integration).

• Knowledge on external vendor tools for design and layout process, and many internal tool and scripts.

• Scripting (Perl/TCL/BASH) and LINUX© environment, net batch and interactive server usage.

• Top-secret and Confidential process information handling.
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Physical Design Engineer

Software Engineer

Process / Project owner

Manager
Computer Science Engineer: DA (Design Automation).

External-vendor tools are designed to be used by many design companies. DA team sync and configure software to meet internal project requirements

- New technology requires many internal development to solve industry delay.
- Some rules and patterns are intellectual property, must keep internal only.

New tools for custom or internal methodologies development.

Process automation:

- Design process, such as synthesis, placement, routing and DR rules cannot rely on manual effort only, to meet time to market plans.
DA qualifications

✓ Understanding of process and project specifics, to develop utilities and solve automation issues.

✓ Higher Scripting skills (Perl, TCL, bash, C, oriented-object, web technologies) as well industry related languages (Verilog, DEF, vendor software).

✓ Project management and system development life cycle.

✓ Top-secret and Confidential process information handling.

✓ Process analysis, optimization and continuous improvement.
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Project and Process Owners (POs)

Before a project is launched;

- POs defines Project methodology, to be followed by SD/LV teams.
- Execute pioneering tasks to evaluate and propose solutions.

In charge on many project technical day-to-day activities:

- Solve project issues, and acts as main contact among several horizontal teams
- Solve corner cases for any block under cleanup or design.

Experienced team members:

- Drives many product activities across multiple geographies, such as full chip integration, final reviews and usually, are the ones delivering the databases to factory.
- Main contact with other Intel design centers when the product needs to be converged.
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People / Project managers

• Set goals and define how success is measured.
• Plan, organize, and monitor the work.
• Maintain focus on continuous improvement of processes, methodologies, and looking for improvements.
• Standardize the work model and checklist further.
• Shape business direction using data and judgment.
• Build the team needed to deliver the results required, keep great place to work.