Development of 3D Through Silicon Stack (TSS) Assembly for Wide IO Memory to Logic Devices Integration

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Agenda / Outline / Overview

- Why 3D for mobile device?
- TSS Demonstrators
- Technical Discussion
- Summary & Conclusions
# 3D Package options

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<th>Device</th>
<th>Current Configurations</th>
<th>TSV configurations</th>
<th>Market Status</th>
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<tr>
<td>Memory</td>
<td>Memory or Memory + Control logic</td>
<td><a href="SCSP.jpg">Image</a></td>
<td><a href="TSV.jpg">Image</a></td>
<td>Development</td>
</tr>
<tr>
<td>Mobile Device</td>
<td>DDR + AP</td>
<td><a href="PoP.jpg">Image</a></td>
<td><a href="TSV.jpg">Image</a></td>
<td>Development</td>
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<tr>
<td>Game console</td>
<td>DDR + GPU/CPU</td>
<td><a href="MCP.jpg">Image</a></td>
<td><a href="TSV.jpg">Image</a></td>
<td>Development</td>
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<td>Logic partitioning</td>
<td>FPGA</td>
<td><a href="FCBGA.jpg">Image</a></td>
<td><a href="TSV.jpg">Image</a></td>
<td>In production</td>
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<td>MEMS/Sensors/IPD</td>
<td>IPD/Image sensors</td>
<td><a href="IPD.jpg">Image</a></td>
<td><a href="TSV.jpg">Image</a></td>
<td>In production</td>
</tr>
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</table>
Why 3D for Mobile Product?

- Multiple 3D Stacking Technologies:
  - PoP based
  - Wire Bond based
  - **3D TSS or Interposer**

- All 3D Technologies *Possibly* Provide:
  - Better form factor
  - Better performance
  - Higher system modularity

- But do you want more *Thin, HD, HP with Long live battery from the Mobile Devices*?*

- High Density TSS Integration can provide the solutions
  - Non TSV LPDDR (x32) solution has limitation to provide required IOs for high bandwidth and power needs
  - Selected Wide IO Memory (>x512) on Logic
    - Lower power consumption and higher bandwidth by low operation frequency per data bit by parallel data processing
  - Practically cannot be deployed w/o TSS technology
High Density TSS Progress

- Small diameter (~5um) high aspect ratio (~10:1) thru silicon via (TSV)
- Via-middle process flow (TSV formation after FEOL)
- High density (10’s um pitch) tier to tier microbump connections
- >1000’s of TSVs & microbumps per chip
- Includes design and test enablement, tools, & methodologies
- Component level reliability & EM
TSS Integrated Demonstrators

NEW MODULES
• High density TSVs
• Microbump interconnect
• Ultra low CTE substrate

INTEGRATION
• Via-middle
• Multi thin die stacking
• Die to Substrate
## Manufacturing Flow Options

<table>
<thead>
<tr>
<th>Chip Stack Flow</th>
<th>Throughput</th>
<th>Die size mismatch</th>
<th>Wafer yield Sensitivity</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>W2W</td>
<td>High</td>
<td>Not allowed</td>
<td>High</td>
<td></td>
</tr>
<tr>
<td>D2W</td>
<td>Low</td>
<td>Limited (top die &lt; bottom die)</td>
<td>Low</td>
<td>WLUF for high UPH</td>
</tr>
<tr>
<td>D2D or D2S</td>
<td>Med</td>
<td>Allowed</td>
<td>Low</td>
<td></td>
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</tbody>
</table>

D2S option was finally selected due to its relatively higher throughput and its ability to accommodate different memory die size.
TSS Process Flow

FEOL
- Via Formation
- Liner Deposition
- Metal Fill
- BEOL

MEOL
- C4 / u-bump pad
- Temporary Bonding
- TSV Reveal / UBM
- Bumping

ASSY - D2S
- Wafer Saw
- Tier 1 Attach
- Tier 2 Attach
- BGA
TSS Technical Challenges – Module process

- Robust TSV formation
  - Via fill, Liner integrity, Cu pumping
- Backside wafer process
  - TSV reveal, pad/bump quality
- Joint metallurgy optimization
  - Yield, EM, thermo mechanical reliability
- Temporary bonding/debonding
  - Thermal budget, No residue demount, TTV
- Chip Attach & UF
  - Warpage control/Tight UF dispense keep out/Yield
- Tier 2 Bonding
  - UPH improve, Filler trap, alignment

- No significant intrinsic issues identified and achieved considerable progress
Adhesive Requirements

- Process compatibility for MEOL BEOL
  - High Temp Resistance
  - Chemical Resistance
  - Mechanical strength during process
- Low out-gassing and residue free release
- Low TTV and Low stress for the bumps
- Low cost
# Temp. Bond/Debond

<table>
<thead>
<tr>
<th>Carrier Compatibility</th>
<th>Thermal Cure + Thermal Slide</th>
<th>Thermal Cure + R.T. Mechanical Slide demount</th>
<th>Thermal cure + Laser Release + Chemical cleaning</th>
<th>UV Cure + Laser Release</th>
</tr>
</thead>
<tbody>
<tr>
<td>Glass / Si</td>
<td>Glass / Si</td>
<td>Glass / Si</td>
<td>Glass / Si</td>
<td>Glass</td>
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</tbody>
</table>

**Bonding**

- Spin Coat Adhesive
- Data Adhesive
- Wafer Conditioning

**Debonding**

- Secure with Chuck
- Thermal Slide Debond
- Clean
- Attached to Dicing Frame
- Remove Carrier
- Rinse
- Peel Adhesive
- Processed Wafer on Frame

**Note**

- Bond Temp < 200C
- Debond < 200C
- Bond Temp < 200C
- Debond: R.T.
- Bond Temp: UV
- Debond: R.T.

**Good progress to accommodate process requirements**
TSS Technical Challenges – Integration

- Thin wafer shipping/handling
  - Difficult to address exact damage initiation points → Possible liability issue
  - Tape-mount process integrity (tape wrinkles, bubbles) improvement
  - Carrier improvement implemented
    - Multiple wafers on the film
    - Effectively suppressing wafer bending
  - Gap: Still not enough damage detection resolution
Shadow moire warpage measurement data of different substrate designs and chip attach condition.

Optimized condition showed more than 30% warpage improvement over non optimized condition.
TSS Technical Challenges – Integration

- Memory MPGA stacking
  - To achieve 40um pitch of 25um diameter Cu pillar bonding, thermal compression bonding method implemented

- Clear relationship btw Bottom die warpage and D2D gap uniformity
- It is very important to maintain tier 1 flatness and optimized Cu pillar bump structure to ensure TC bonding yield
### Package Material Impact on Device

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Tg</th>
<th>CTE 1 (&lt;Tg) ppm</th>
<th>Modulus (&lt;Tg) GPa</th>
<th>Normalize Mobility change</th>
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</thead>
<tbody>
<tr>
<td>NCP</td>
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<tr>
<td>Default</td>
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</table>

- Mold compound showed biggest mobility swing by all three material properties corner values while NCP is mainly sensitive to CTE corner values.
- Material selection, device size, stacking location of both devices and total TSS package form factor must be carefully optimized.
Failure bit counts increase by increasing refresh time as expected but first failure of each test unit is passed the 64 millisecond spec with big margin.
Reliability

- TSS package exceeds typical reliability requirement and maintain joint integrity

Microbump resistance measurement data of (a) temperature cycle B (TCB), (b) high temperature storage (HTS), Cross-sectional microbump image of (c) 1000 cycles of TCB and (d) 1000 hours of HTS
Summary

- Presented TSS package development work and successfully demonstrated integration of up to 4 die memory MPGA on the logic device
- Technical challenges and their mitigation efforts were discussed
- This paper suggested no major technology road block to enable TSS technology for mobile product
- This disruptive technology to the volume production will depend on not only technical progress but also business aspect of value propositioning