3D TSV IC MANUFACTURING CHALLENGES: TEMPORARY AND PERMANENT BONDING TECHNOLOGIES

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Outline

• Introduction:
  • 3D IC Package Technology Trends: Stacked die CSP, Package-on-Package (PoP), 3D TSV Die Stack Technologies

• 3D TSV IC manufacturing technology challenges, solutions and opportunities:
  • 3D TSV IC Integration flows
  • Temporary bonding & de-bonding technology
  • Permanent bonding technology
  • Wafer level pre-applied conductive adhesive materials for 3D TSV die stack opportunities

• Summary
3D Advanced Packaging: Die, Wafer, Package Stack

**Package stacking**
- 1. PiP packages (Package in Package)
- 2. PoP packages (Package on Package)
  -> Rather OSATs

**Die stacking**
- Wire Bonding

**Wafer stacking**
- 3D IC w/ TSV

Source: Yole Development

“Edge-of-Silicon” Interconnect Source: Vertical Circuits, Inc
3D Package Trends: Stacked Die CSP

Stacked die in a package is common for more functionality in small footprint.

System In Package

- NOR+RAM+ NAND+uC

2 Die Products
- 150um Die
  - Wafer Dicing vs. Moisture/Temp Reliability

3 Die Products
- 125um Die

4 Die Products
- 100um Die

5-8 Die Products
- 50 - 75um Die
  - Ultra-Thin Die Handling vs. Die Cracking
  - 2nd Gen Wafer Dicing vs. Moisture/Temp Reliability
  - 2nd Gen Materials vs. Package Stress

SCSP
- Four Die Stacked Memory with One Spacer Die

PoP
- Top; Three Die Stacked Memory
- Bottom; Single Die Digital Baseband
3D Package Trends: PoP Technology

2008 2009 2010 2011 2012

M+L Die Stacking
Lower Cost

Smaller Form Factors
Oppty’s for Modularization...
Memory + Logic + ?

Going Below 0.5 pitch

Modules/Systems in Package

Strong Z height Reduction for PoP Top package
- Die Thinning
- Die Attach Thickness
- Thin Core Substrates
- 0.5 => 0.4 mm => 0.35/0.3 mm pitch
- Tighter Warpage Control

Enabling Higher I/O and Further X-Y Reduction
Current High Density 2.5D/3D TSV Applications and Outlook

<table>
<thead>
<tr>
<th>2.5D Hi Perf</th>
<th>Side by side die stacked on a passive interposer that includes TSVs &amp; high density RDL. <em>Ex: FPGA, Server, GPU, Network Processor</em></th>
</tr>
</thead>
<tbody>
<tr>
<td>3D Memory</td>
<td>Multiple DRAM die stacked standalone or on a memory controller chip. <em>Ex: WIO1, WIO2, HMC, HBM</em></td>
</tr>
<tr>
<td>3D Memory on Logic</td>
<td>One or More DRAM die stacked directly on processor die (<em>M-O-L</em>) (or <em>L-O-M</em> for high power processors)</td>
</tr>
</tbody>
</table>

Current/ near future (2012 - 2014)
- Interposer products
- Wide IO DRAM

- Heterogeneous integration (beyond memory on logic)
- Higher (>> 5 stacking levels)
- Smaller (<< 5 micron width, >> 10 aspect ratio)

Far future (2017 - 2025)
- Beyond CMOS (photonics, sensors, etc)
Comparison Wide IO Application Between Mobile and Computing/switch (High Performance)

<table>
<thead>
<tr>
<th></th>
<th>Computing Wide IO (High Performance)</th>
<th>Mobile Wide IO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Structure Limitation</td>
<td>Thermal</td>
<td>Package Height (&lt;1 mm)</td>
</tr>
<tr>
<td>Cost</td>
<td>Dependent on design, technology and cooling technique</td>
<td>Serious</td>
</tr>
<tr>
<td>Data Band Width (Speed)</td>
<td>&gt; 64GB (512G bps)</td>
<td>&gt; 12GB</td>
</tr>
<tr>
<td>Power</td>
<td>10-150W</td>
<td>&lt; 3W</td>
</tr>
<tr>
<td>Interposer</td>
<td>Can be used</td>
<td>Not Use</td>
</tr>
<tr>
<td>Structure for Thermal</td>
<td>Use Heat Sink and TIM: Liquid</td>
<td>-</td>
</tr>
<tr>
<td>Structure</td>
<td><img src="image" alt="Diagram" /></td>
<td><img src="image" alt="Diagram" /></td>
</tr>
</tbody>
</table>
Assembly Process Flow: 3D Logic + memory

- Case 1: Logic TSV die (DtS) => Memory cube to Logic TSV (DtD) => Backend (Molding/BA/singulation)
  - Logic die w/NCF (C4 bump face down)
  - C4 process for Tier 1
  - Memory Die (or cube) to Logic die attach process (T/C bonding)

- Case 2: Memory cube to Logic TSV die (DtD or DtW) => Stacked Memory cube + Logic to sub => Backend (Molding/BA/singulation)
  - Memory die (or cube) to Logic die (or wafer) (reflow or T/C bonding + CUF)
  - Wafer level mold and singulation (optional for DtW)
  - Stacked Memory + Logic die to substrate attach process (C4 bonding + CUF)
Assembly Process Flows: 2.5D TSI

**Case 1**: Logic die and memory die/cube attach to Interposer die (or wafer) (DtI) -> WLM (optional) -> Interposer Stack attached to Substrate (DtS) -> Backend (head sink attach/marking/ball attach/flux clean)

- Logic Die
- Memory Die (cube)
- TSI die (or wafer)
- DtID (or DtIW) + UF
- DtS + UF
- Heat sink (option)
- Backend

**Case 2**: Interposer attached to Substrate (DtS) -> Logic die and memory die/cube attach to Si Interposer (DtI) -> Backend (head sink attach/marking/ball attach/flux clean)

- TSI die
- Logic Die
- Memory
- PKG Substrate
- DtS + UF
- DtID + UF

**Abbreviations**:
- DtID: Die to Interposer Die
- DtIW: Die to Interposer Wafer
- DtS: Die to Substrate
# 2.5D/3D TSV IC Interconnect Trend

**Mobile wide IO Memory + Logic 3D TSV**

**Memory and Logic on 2.5D TSI**

![Diagram](source: SEMATECH)

<table>
<thead>
<tr>
<th></th>
<th>Mobile Wide IO</th>
<th>2.5D TSI for High Performance Computational wide I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2013</td>
<td>2015</td>
</tr>
<tr>
<td>Total power (W)</td>
<td>Max.12</td>
<td>Max.16</td>
</tr>
<tr>
<td># of I/O interconnect (M-L and M-Interposer)</td>
<td>Max. 10000</td>
<td>Max.12000</td>
</tr>
<tr>
<td>Micro-bump pitch (um)</td>
<td>40</td>
<td>30</td>
</tr>
<tr>
<td>Logic die thickness (um)</td>
<td>Min. 50 um</td>
<td>Min. 30 um</td>
</tr>
<tr>
<td>Memory cube thickness-4 die stack case (um)</td>
<td>240-400</td>
<td>240-400</td>
</tr>
<tr>
<td>M-L gap thickness (um)</td>
<td>15-30</td>
<td>10-25</td>
</tr>
<tr>
<td>Interposer size (mm)</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
Fine Pitch Interconnect Demand

Source: Globalfoundries
TSI Principal Architecture: Key Challenges

**Wafer thinning technologies**
- Grinding
- CMP
- Plasma
- Wet etching
- TSV nailing techniques

**TSV formation**
- TSV patterning
- TSV etching (low scalloping, low undercut)
- TSV isolation/seed/barrier: conformal and continuous deposition
- TSV filling: voidless deposition, CMP uniformity

**Wafer handling**
- Temporary bonder/debonder
- Carrier wafer (glass / silicon)
- Temporary bonding materials

**Bonding / Assembly**
- C2W and W2W bonding
- Inter-die connections (bumps, Copper pillars, etc.)
- Bonding materials & Underfill (pre-applied UF, CUF, WLUF...)

**Source:** Yole Development
**Material & Process Challenges**

**Permanent Bonding (3), (7):**
- Compatibility with low k dielectric
- Solder micro-bumping
  - Scalable pitch & high density
  - Low stress bonding

**Underfill (2) (6) & TIM1 Materials (1):**
- Low gap (< 50 micron) filling material & process
- TIM with high thermal conductivity (> 5W/mK)

**Temporary Bonding (4):**
- Lack of consensus over materials & processes
  - Thermal slide off vs zone debond vs laser release

**TSV Fill Materials and Process (5):**
- Highly reliable, low cost liner/barrier/seed/plate materials
- Scalable materials (Eg; void free from 10 x 100 to 5x50 to 2x40)
Technical Development Focus

• Adhesive Bonding Materials
  – Wafer level NCF and WLUF
  – High thermal conductive UF
  – Photo-definable underfill for ultra-thin gap filling capability <10 um

• Bonding Process
  – Robust thin wafer handling/temporary bonding/backside process
  – Robust DtD, DtW and WtW integrated bonding process
  – Thermo-compression bonding
  – Cu-Cu direct bonding for <20 um pitch

• Wafer Level Molding Materials and Process

• Metrology, Inspection and Test
  – Incoming and shipping standard for thin wafer bonded pair and memory TSV stack cube, etc
  – TSV module, backside integration and Assembly module inline inspection metrology (TSV void, adhesive void, bump uniformity, underfill void, surface inspection, etc)
General Thin Wafer Backside Process

1. Clean (Memory/TEG wafer)
2. Photoresist (PR), develop, clean, oxide mask patterning, DRIE, PR strip, remove oxide mask, clean
3. SiO₂/barrier/seed layer deposition
4. PR Patterning for plating, Cu or Ta plating, PR & seed layer removal
5. Residual Cu CMP
6. Front-side metallization/UBM
7. Support wafer (temporary) bonding
8. Via exposing by wafer thinning
10. Wafer micro-bumping
11. De-bonding support wafer, Clean
12. C2C or C2W bonding

Source: ITRI
Supply Chain and Business Model Challenges

- No standard for supply chain flows
- Many integration models
- Cost vs performance

Source: J. Greenwood, GIT2012
**Why Temporary Bond?**

- Wafers becomes flexible after thinning.
- Wafers are easy to crack without wafer support.
- A lot of process being done after wafer thinning.
- Wafer support system is needed for 3D Integration.

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**source: ITRI**

**source: Yole**
Temporary Bonding Process Options and Key Issues for DtD and DtW

Process Flow:
- Carrier wafer: Glass or Si
- Adhesive coating: Spin coating, Bake
- Wafer bonding: T/T/P
- TSV process: Back-grind, Cu reveal, Passivation, Planarization, RDL/Bumping
- Dicing tape transfer: Lamination
- De-bonding: De-bonding, Thermal/chemical/UV laser release, Cleaning

Issues:
- Thickness tolerance
- No residual solvent
- Void free
- Alignment
- Large TTV & chipping
- Side etching
- Delamination
- Void & Delamination
- Warpage
- Void & Delamination
- UV layer damage
- Residue

Dicing after de-bond
Dicing before de-bond
Dicing Before Grinding (DBG)
Typical Temporary Adhesive Layer and TSV Defects

- Bubble/contamination after glue coating and after bonding
- Post grinding defect/dimple => TSV exposure
- TTV and Warp/Bow control

Source: Nanda Tech

Table:

<table>
<thead>
<tr>
<th>Layer</th>
<th>Bow (um)</th>
<th>Warp (um)</th>
<th>Average Thickness (um)</th>
<th>TTV (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>All</td>
<td>-328.706</td>
<td>375.119</td>
<td>1509.816</td>
<td>13.865</td>
</tr>
<tr>
<td>Si</td>
<td>779,947</td>
<td>&lt;1um</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Glue + Glass</td>
<td>729.869</td>
<td>14.858</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bow/Warp

TTV Glue + Glass

Source: Nanda Tech
### Temporary Bond Process Flow Issues

<table>
<thead>
<tr>
<th>ISSUE / CHALLENGE</th>
<th>APPLY</th>
<th>ALIGN &amp; BOND</th>
<th>WAFER PAIR PROCESSING</th>
<th>DEBOND</th>
<th>CLEAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness</td>
<td>Thickness</td>
<td>&lt; 10 um</td>
<td>up to what max. temp?</td>
<td>Room Temp?</td>
<td>C4 or ubump?</td>
</tr>
<tr>
<td>Uniformity</td>
<td>Uniformity</td>
<td>Room Temp?</td>
<td>Bond Strength</td>
<td>Method</td>
<td>Cleaning</td>
</tr>
<tr>
<td>Thermal</td>
<td>Thermal</td>
<td>Bond Strength</td>
<td>Chemicals</td>
<td>Throughput</td>
<td>Chemical</td>
</tr>
<tr>
<td>UV</td>
<td>UV</td>
<td>Grind/polish</td>
<td>Mechanical</td>
<td></td>
<td>at dicing tape?</td>
</tr>
<tr>
<td>Combination</td>
<td>Combination</td>
<td>Handling</td>
<td>Chemical</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**METHODS**

- Spin coat
- Laminate
- Zone
- Combination

- Thermal
- UV
- Combination

- Thermal
- UV / Laser
- Mechanical
- Chemical
- Zone

- Spray
- Immersion
- Plasma
- Combination

- Broad range of process conditions depending on materials and bonding/de-bonding methods
  1. Bonding method: thermal (High, Medium or Low temperature) or UV or others?
  2. De-bonding method: Room to Low, Medium or High temperature de-bonding?
  3. Adhesive thickness: any thickness guideline?
  4. Thermal stability and residual wafer stress during TSV backside processes and permanent bonding
  5. Where to release and cleaning method??
  6. Cost and throughput
Temporary Bonding/De-bonding Adhesive Materials/Equipment

Scope

Coating
- Spin coat & bake
  - HT1010, 9001A, HD3007, X5610 -> spin coating only @carrier wafer
  - 3M WSS, TZNR-A -> spin coating both TSV & carrier wafers
  - T-MAT -> spin coating + PECVD @TSV side, elastomer coating on carrier side
- Thermal bond/UV
  - • EVG
  - • Suss
  - • TOK
- Align/Bond

De-bonding
- (a) Thermal slide off
  - • EVG
  - • Suss
  - HT1010, 9001A HD3007 X5610, TA3000
  - Adhesive specific cleaner
  - Dipping/spraying & drying
- (b) UV/laser release
  - • Suss/Tazmo
  - 3M WSS
  - No chemical cleaning
- (c) Mechanical release
  - • Suss
  - T-MAT
  - Cleaning & Drying
- (d) Chemical release
  - • TOK
  - Zero-newton adhesive
  - Cleaning stripper
- (e) Zone release
  - • EVG/Brewer
  - ZoneBOND™
  - Cleaning stripper

Cleaning
TB/DB Material & Process Landscape

Debond Process
- Zone Debond
- Thermal Slide-off
- Chemical de-bond
- Mechanical de-bond
- Laser De-bond

Adhesives
- DuPont
- Sumitomo Bakelite
- Nitto Denko
- Brewer Science
- TOK
- ShinEtsu MicroSi
- Suss/TMAT
- 3M
- JSR Micro

Source: Sematech
TB/DB Technology Comparison

- High throughput and no damage at device wafer
- Low cost adhesive, carrier wafer including recycle-ability and machine
- High thermal stability and room temperature de-bonding process

<table>
<thead>
<tr>
<th>Method</th>
<th>Thermal</th>
<th>Zone</th>
<th>Laser</th>
<th>Chemical</th>
<th>Wedge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Machine</td>
<td>EVG, TEL, Suss</td>
<td>EVG, Suss</td>
<td>TAZMO, Yushin, Suss</td>
<td>TOK</td>
<td>Suss</td>
</tr>
<tr>
<td>Material</td>
<td>BSI, ShinEtsu, Sumitomo</td>
<td>BSI, ShinEtsu, Sumitomo</td>
<td>3M</td>
<td>TOK</td>
<td>TMAT, Dow</td>
</tr>
<tr>
<td>Machine price</td>
<td>Middle</td>
<td>High</td>
<td>Middle</td>
<td>Middle</td>
<td>High</td>
</tr>
<tr>
<td>Material price</td>
<td>High</td>
<td>High</td>
<td>Middle</td>
<td>High</td>
<td>Middle</td>
</tr>
<tr>
<td>TTV</td>
<td>Good</td>
<td>Normal</td>
<td>Good</td>
<td>Normal</td>
<td>Normal</td>
</tr>
<tr>
<td>UPH</td>
<td>Middle</td>
<td>Low</td>
<td>High</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>

Source: Amkor
Assembly & Stacking Strategy for 2.5D/3D

- High throughput and reliable stacking solutions needed

- Various assembly integration possible, dependent on FtF or FtB, number of die stacks, die size difference, die thickness, etc.

- For 2.5D interposer & 3D IC stack, Chip to chip for OSAT, chip to wafer for foundry preferred.

<table>
<thead>
<tr>
<th>Category</th>
<th>Chip to Chip</th>
<th>Chip to Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schematic</td>
<td><img src="image" alt="Chip to Chip Schematic" /></td>
<td><img src="image" alt="Chip to Wafer Schematic" /></td>
</tr>
<tr>
<td>Process</td>
<td>Chip to Sub =&gt; Chip to Chip</td>
<td>Chip to Chip =&gt; Chip to Substrate</td>
</tr>
<tr>
<td>Advantages</td>
<td>Standard OSAT flow</td>
<td>Mitigate die to interposer yield concern</td>
</tr>
<tr>
<td>Challenges</td>
<td>Substrate warpage after interposer may impact on micro-bump joint yield btw top die to bottom interposer</td>
<td>Handling of thin die with FC bump and micro-bump, and die stacking on temporary carrier or stage</td>
</tr>
</tbody>
</table>
## Bonding Pitch and Methods for 2.5D/3D IC

<table>
<thead>
<tr>
<th>Category</th>
<th>Bonding Path</th>
<th>Bonding Structure</th>
<th>Pitch</th>
<th>Process/Flux/UF</th>
<th>Bonding Accuracy</th>
<th>Application</th>
</tr>
</thead>
</table>
| **Solder Bumps** (Metal becomes liquid during bonding process) | C4 FC (Controlled Collapse Chip Connect)         | >130um (Normal)   | - Cold solder FC Process  
  - Flux dipping & mass reflow  
  - Capillary UF             | 10 um @3sigma                                         | DtS              |
|                           | C2 FC (Chip Connect)                             | >60 um (Fine pitch) | - Cold Cu-pillar FC Process  
  - Flux dipping & mass reflow  
  - Capillary UF or molded UF | 6 um @3sigma                                        | DtS, DtD, DtW  |
|                           | TC/LR FC (thermo-compression/Local Reflow)       | >40 um (Ultra fine pitch) | - Hot Cu-pillar FC Process  
  - No flux, TC/LR  
  - Pre-applied NCP/NCF or Capillary UF | 2-3 um @ 3 sigma                                        | DtS (for large die case), DtD, DtW |
| **Solid State Diffusion** (Metal remains solid during bonding process) | Cu-Cu Direct Bonding                              | < 20 um           | - Cu-Cu TC bonding (SAM, nano-rod assisted)  
  - Insertion bonding  
  - Direct bonding  
  - No flux  
  - No UF or <10um narrow gap UF | 1 um @ 3 sigma                                        | DtD, DtW, WtW  |
3D TSV Die Stack: Bonding Technology Challenges

- **TSV Process Flow:**
  - Via-middle process and Cu/Sn eutectic T/C bonding

![Diagram of TSV process flow](source)

- **Assembly BE process:** capillary UF and molding or molded-UF
  - **Capillary UF’s limitation**
    - The difficulty to flow a liquid in a small gap. Current limit is considered around 80μm.
    - The difficulty to reach gap between top and bottom die
    - The difficulty to approach needle between stacked die on the substrate wafer
  - **MUF limitation:** very expensive, gap limitation
Key Challenges for Gap filling and High Thermal Conductivity

Source: Sematech

- Thermal Conductivity (≥ x2)
- Geometrical Challenges (x3)
- Current POR Underfill (capillary UF)
- Interposer with ~ AR=1500 (30mm die / 20um gap)
- AR=500 (25mm die / 50um gap)
- AR=1500 (30mm die / 20um gap)

Nano-material filler
Alumina filler
Silica filler
Permanent Bonding (Gap filling) Materials

- High throughput and reliable materials needed
- Fine gap filling CUF LVM, NCP/NCF under development, dielectric together with Cu-Cu bonding under research

<table>
<thead>
<tr>
<th>Material</th>
<th>Chip level</th>
<th>Wafer level</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CUF</td>
<td>NCP</td>
</tr>
<tr>
<td>Method</td>
<td>Filling after bonding</td>
<td>Pre-applied under-fill</td>
</tr>
<tr>
<td>Throughput</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Reliability</td>
<td>High</td>
<td>Medium</td>
</tr>
<tr>
<td>Overflow</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Small gap</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>High stack</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>
WL-Underfill Technology for 3D IC Stack

• Conventional WL-UF flip chip process flow

• WL-UF is very attractive technology for 3D TSV D2D/D2W bonding and under development in major 3D research activities; some of challenges as below
  – Needs solder reflow for the solder cap on Cu bump and this can lead to temporary carrier bonding quality degradation.
  – Still WL-UF material under development.
  – Special attention to UF voids formation and bleeding after stacking.
  – High process time for TC bonding
TSV Die Stacking Process by WL-ACF/NCF

Wafer TSVed → Cu bump → TSV

Wafer TSVed → ACF/NCF → Cu bump → ACF/NCF lamination → Wafer singulation

Die pick up → Die attach process for die 1 → Die attach process for die 2+ → Molding

Flip Chip Bonding Process by WL-ACF

- ACF (B-stage) lamination
- Dicing along dot-lines (scribe lines)
- Non-solder bump
- Si chip
- Substrate
- Force & Heat

- Minimizing of voids
- No moisture absorption
- No ACF delamination
- No changes of ACF material properties
- Stable bump contact
- No ACF voids by ACF flow
- Sufficient fillet formation

Highly Thermal Gap Filling Material

Source: Namics Corporation

3x thermally conductive UF can improve current carrying capability, and reduce junction temperature.

Wafer level Mold Materials for 2.5D/3D TSV IC Applications

- CoWoS is proposed as foundry turn key model.
- Wafer level mold process is one of key unit process in CoWoS.
- Wafer level mold material is dispensed on CoW wafer then molding, curing and dicing process done.

Source: TSMC
Wafer Level Molding Materials & Processes

Die to Wafer Molding Process
- Molding after wafer thinning
- Molding before wafer thinning

Suppliers development status:

<table>
<thead>
<tr>
<th>WL mold materials</th>
<th>Nagase</th>
<th>Hitachi</th>
<th>Sumitomo</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>liquid</td>
<td>liquid</td>
<td>Liquid, granule</td>
</tr>
<tr>
<td>High thermal</td>
<td></td>
<td></td>
<td>Under development</td>
</tr>
<tr>
<td>WL mold</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Molding compound should have enough rigidity and thermal stability for after processes and BLR
Optical Interconnect

- Integration is the only way to cut the cost of optical links
- Si Photonics combines the advantage of photonics with CMOS manufacturing

CMOS

- Volume Production
- Low Cost
- High Integration
- Miniaturization

Photonics

- High performance communication
- Low power
- Small size and weight

Si Photonics

- High Integration
- Miniaturization
- Higher Bandwidth
- Lower cost
- Lower power
Si Photonics + 3D TSV

- 3D integration (Cu Pillar & TSV) technology in combination with Si Photonics:
  - Photonic Interposer

  - Based on hybrid integration technology, by adding TSV to the “photonic die”
    - Small area required for IO on ASIC die
    - No change of heat sinking approach, external light sources
    - Electrical interfaces to ASIC through bumps and TSV

- Advantages:
  - Very low system level power (no PHYs for low impedance lines)
  - High density
  - Small form factor
  - Scalable

Source: Luxtera
Summary

- Temporary bonding/de-bonding is a key enabling technology for 2.5D and 3D TSV IC Integration.
  - There are several technology options available, but should improve the capability, performance and cost to cover the industry product requirements as much as possible.
  - Room temperature bonding/de-bonding and high thermal stability are well aligned requirement for temporary bonding adhesives.
- Temporary bonding/de-bonding process should be well aligned with overall 2.5D/3D TSV IC integration strategy including final bond strategy.
  - D2D, D2W or W2W bonding
  - Reflow bonding, or Thermo-compression with and without pre-applied underfill
- TSI development just started for fine pitch interposer application
  - Supply chain strategy: foundry turn key or foundry+OSAT
  - Thin wafer handling will play a key role in delivering the low cost and reliable TSI package.
THANK YOU