Packaging Challenges

Driven By The IoT And Migration To The Cloud

Presented by: W. R. Bottoms

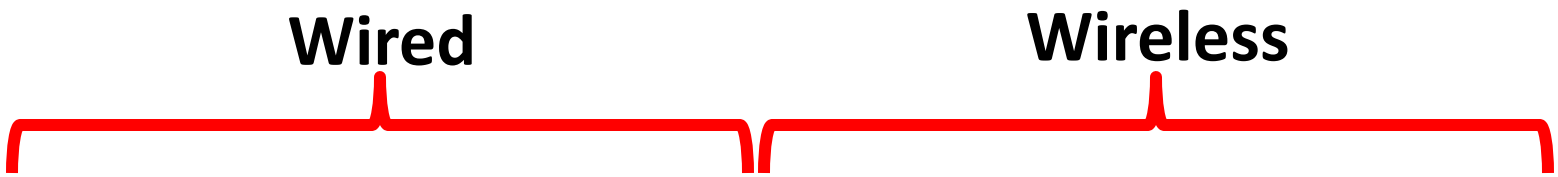
Emerging Technology Drivers

There are 2 market driven trends forcing more fundamental change on the industry as they move into position as the new technology Drivers.

- ✓ **Rise of the Internet of Things**
- ✓ **Data, logic and applications moving to the Cloud**

Over the next 15 years almost everything will change including the global network architecture and all the components incorporated in it or attached to it.

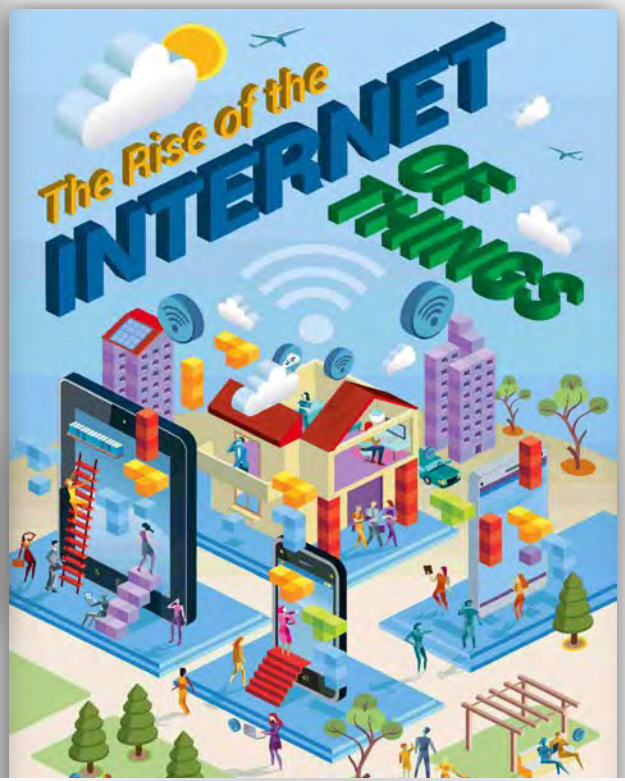
The Driving Forces are Changing



Driver	Mainframe computers	Fixed personal computer	Mobile Consumer	Internet of Things and the Cloud
Key success Parameters	1. Performance 2. Cost	1. Cost 2. Performance	1. Cost 2. Power 3. Performance 4. Size	1. Cost 2. Power 3. Latency 4. Bandwidth density 5. Size

Rise of the Internet of Things

The Internet of Everything
Driven by Human Communication and Machines



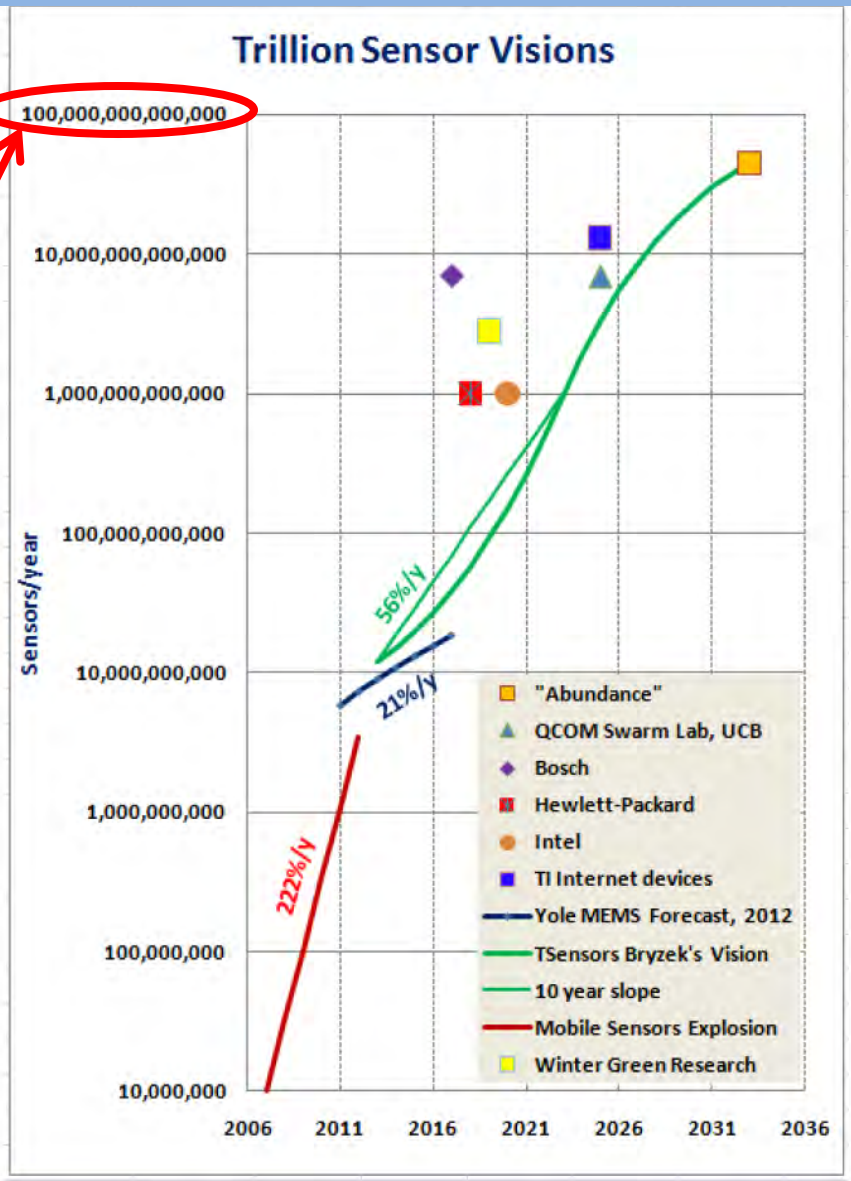
The past 25 years of internet growth was fueled by human communications. The next 25 years will be fueled by machines- much of it by IoT

IoT With Trillions Internet Connected Sensors

The projected growth is likely to be driven by applications yet to be imagined:

- ✓ **Medical**
- ✓ **Industrial**
- ✓ **Agricultural**
- ✓ **????**

100 Trillion



Internet of Things: Technologies Enabling The Revolution

Rules for V-to-V Communication to be released in 2016

Vehicles will "talk" to each other sharing:

- ✓ Vehicle size
- ✓ Position
- ✓ Speed
- ✓ Heading
- ✓ Lateral/longitudinal acceleration
- ✓ Yaw rate
- ✓ Throttle position
- ✓ Brake status
- ✓ Steering angle
- ✓ Wiper status turn signal status
- ✓ Enabling safety/mobility applications.

Source: NHTSA

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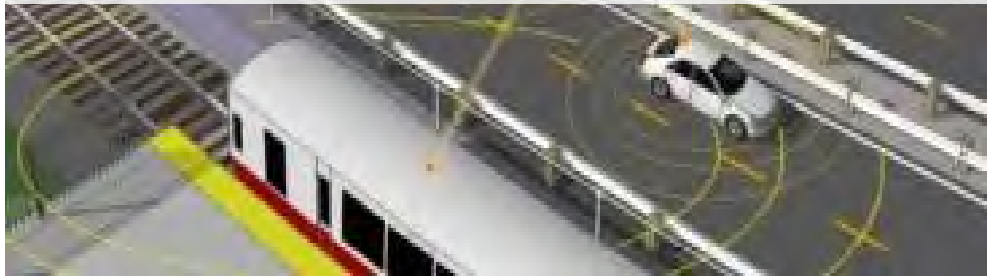
Higher reliability requirements, greater electronic content, heterogeneous integration and a hostile environment

All Expanded Packaging Challenges

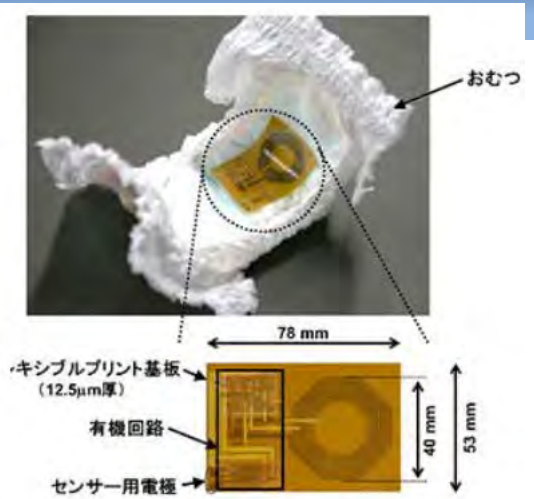


Source: NHTSA

New Connected Products Are Coming

Even diapers will be connected

– 40M/day in the US alone



- Real-time diaper wetness sensor & notification
- Impedance measurement
- RF connection
- University of Tokyo work

Source: www.medgadget.com

Pacemaker in the heart
With smart phone

Many connected products will connect to and through Smart phones and tablets

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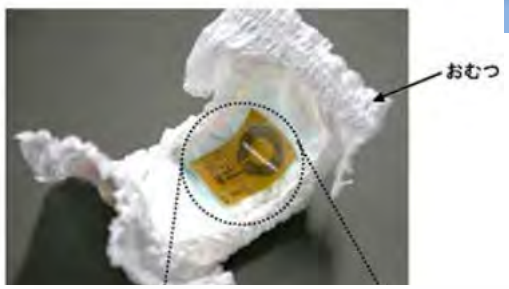
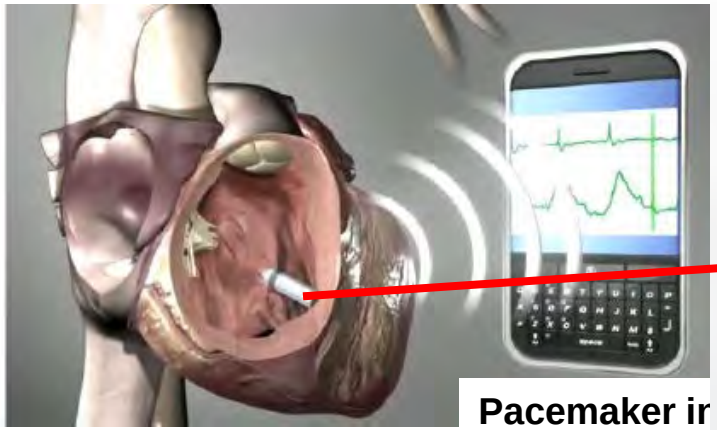




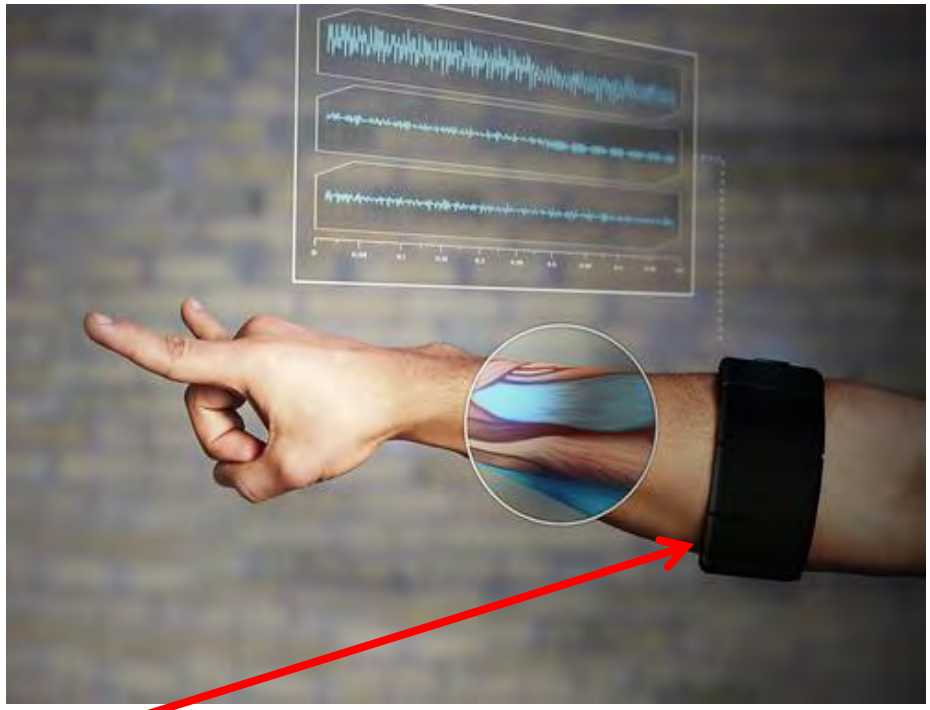
Pacemaker ir
heart
With smart pl

Many connected pro
and through Smart p

Emerging IoT Sensor Applications will Require new Package Architectures

Thalmic working with ***Google Glass***, ***Epson Moverio***, and ***Recon Jet*** already has a half dozen applications ready.

One is for medical applications when a doctor need hands-free, voice free access to information.

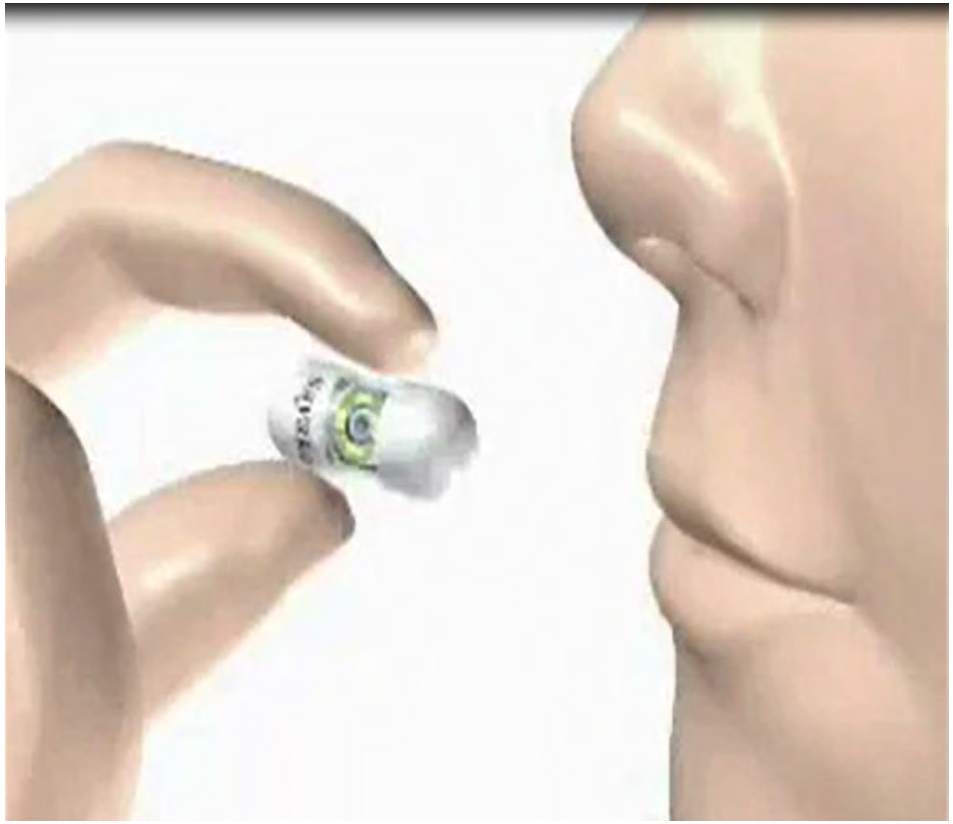


Packaging this wearable with sensors, logic, and communications while keeping it comfortable and reliable adds new packaging challenges

Arm band can discern dozens of hand gestures making head-mounted displays hand and voice free.

Source: Thalmic Labs

IoT Medical Devices



Next Generation Endoscope

Contact Lens with intelligence and control

IoT: Brain Wave Control is here

Emotiv Insight Brainware

- ✓ This product from Philips gives brain wave control of machines to people
- ✓ 3 Probes mounted in a headband
- ✓ Initial application is to give people with Lou Gehrig's Disease control over household appliances and systems.
- ✓ Initial human trials to date have been successful.

Is Man to machine telepathy coming?

The prospect opens the imagination for science fiction to become reality

Source: Philips

Migration to the Cloud
Data, logic and Applications

What are the Packaging Challenges?

Data Traffic Drives Network Requirements
Network Components Drive Packaging

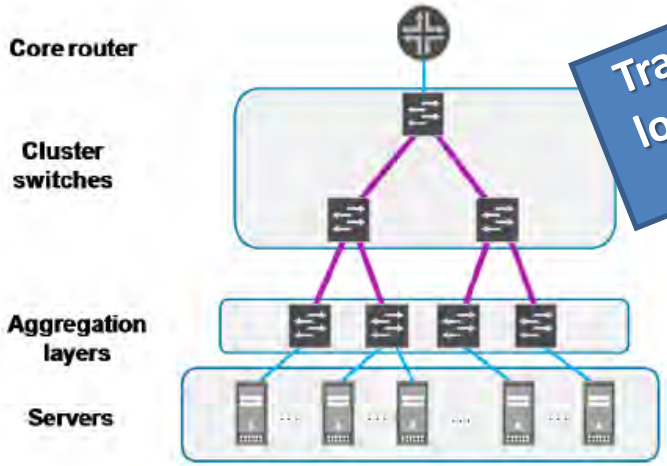
Changes driving data traffic:

- ✓ Global IP traffic will pass 1.4 Zettabytes (10^{21}) by 2017
- ✓ Wireless traffic will surpass wired traffic by 2016
- ✓ The number of mobile-connected devices will exceed the number of people on earth by the end of this year
- ✓ IoT growth will drive demand for bandwidth
- ✓ Data, Logic and Applications are migrating to the Cloud

Today packaging is a limiting factor in cost, performance and size.

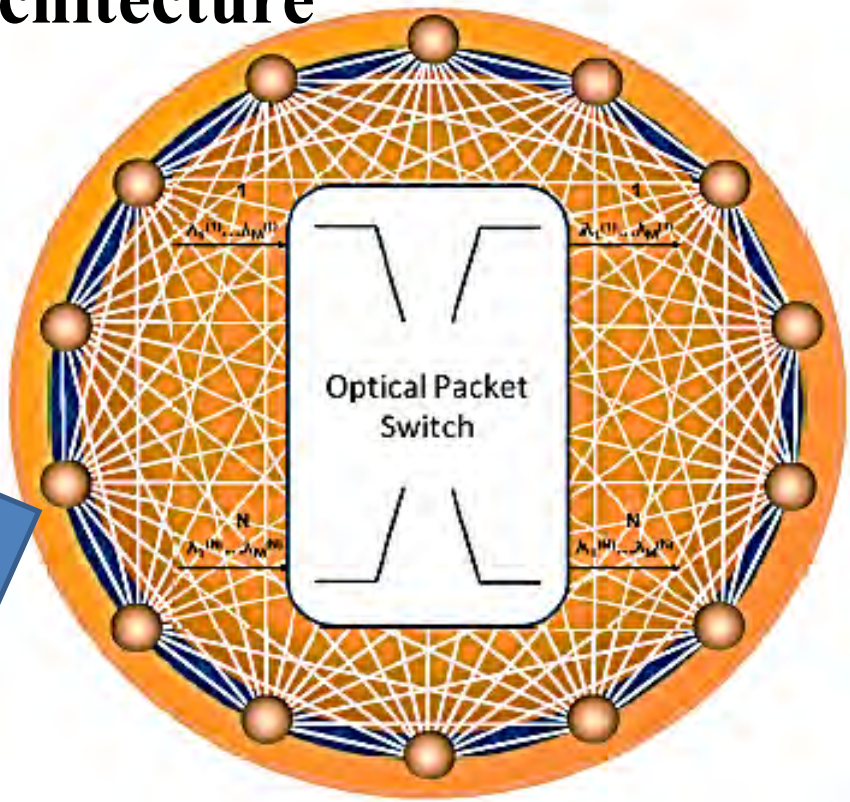
The Network Architecture Must Change Globally and Locally

- ✓ **Higher connectivity Flat Architecture**
- ✓ **Higher bandwidth per port**
- ✓ **Lower end-to-end latency**
- ✓ **Lower power**
- ✓ **Lower cost**



Traditional Hierarchical Tree Topology

Transition to lower Power & latency



Flat Network Topology

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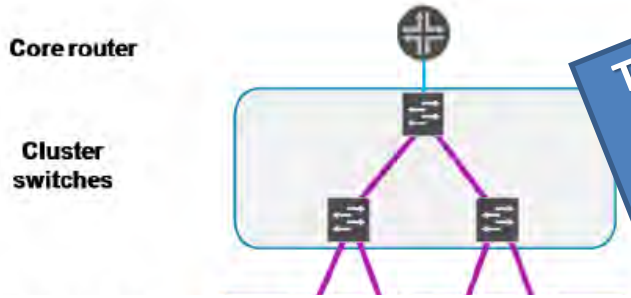
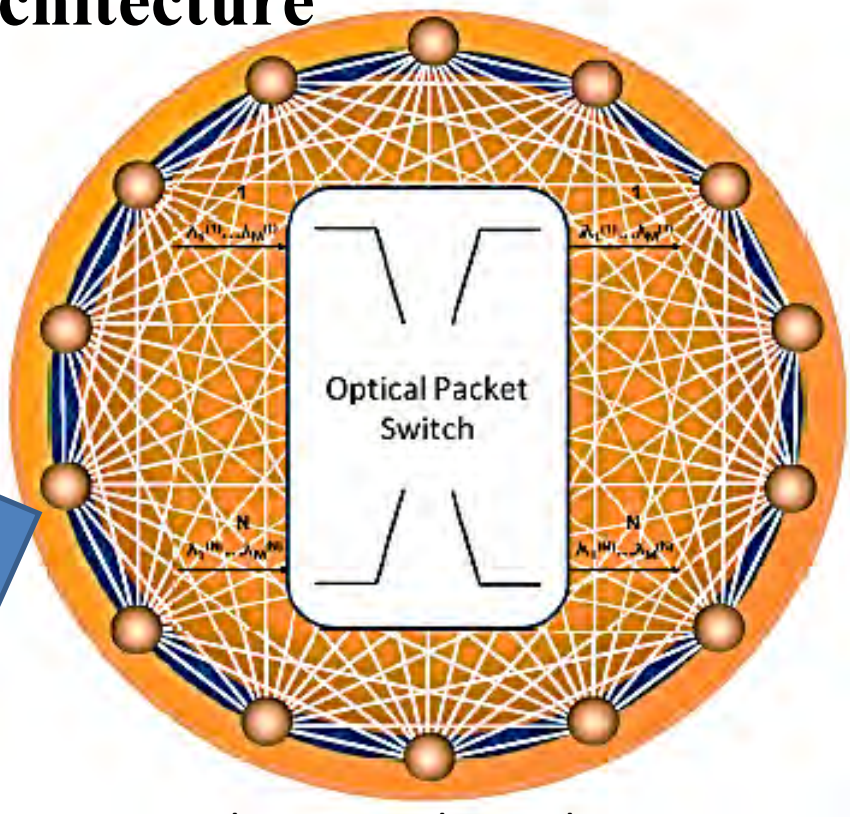


Transition to lower Power & latency



Photonics to the Board, package and even chip level may be required.

The Network Architecture Must Change Globally and Locally

All this is needed at *no increase in total cost and total Network power*.

Power and cost/function need *>10^4* improvement over the next 15 years.

Only a Revolution in Packaging can satisfy these diverse Needs

At the leading edge everything will change including the global network and everything included in it and connected to it. This requires:

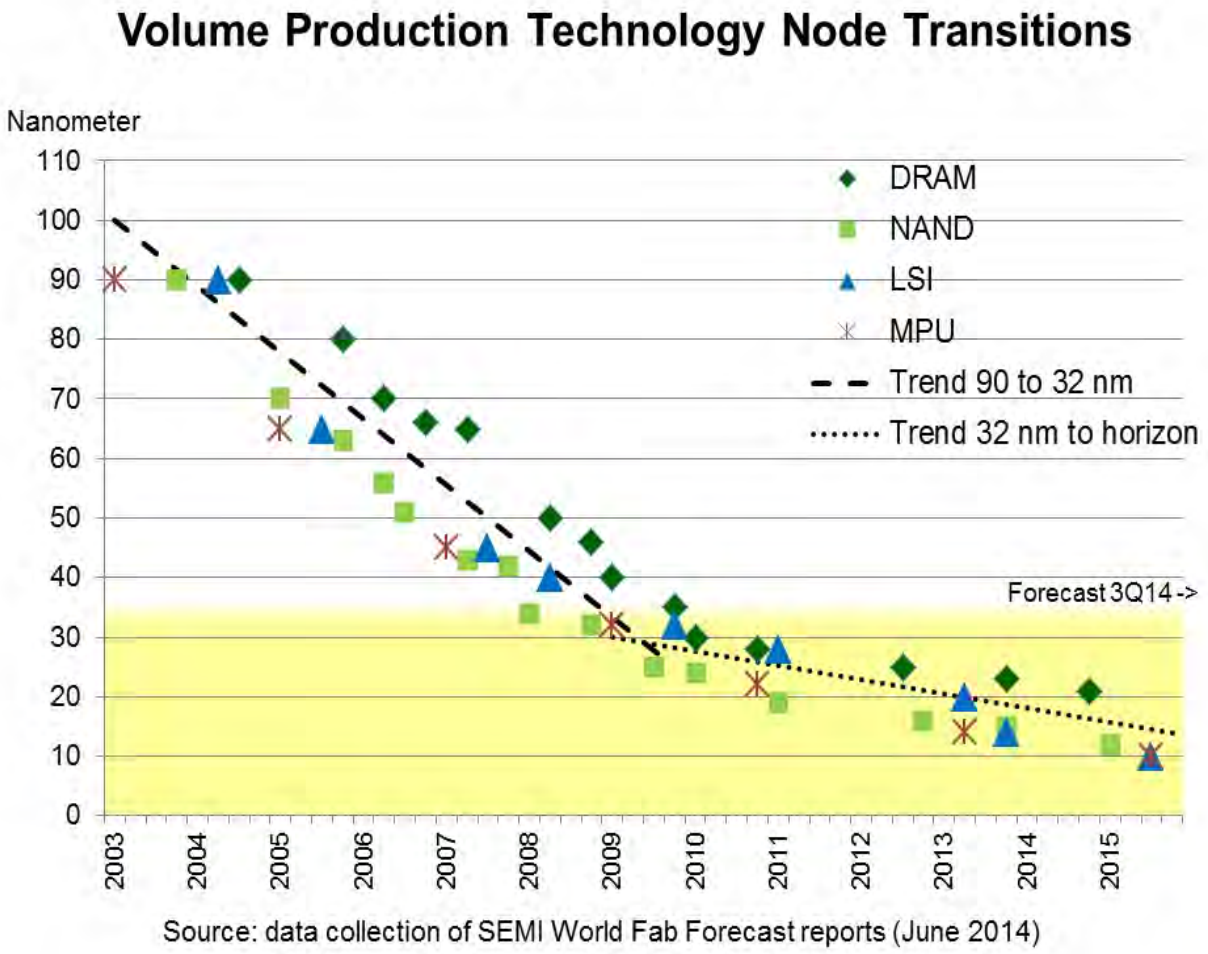
- ✓ New design and simulation tools
- ✓ New materials
- ✓ New device designs and architectures
- ✓ New package architectures
- ✓ New network architectures
- ✓ New manufacturing processes

The Revolution in Packaging

Fab Node Progress is Slowing

In 2016 38% of Production will be at 130ηm first introduced in 2001

Source: SEMI



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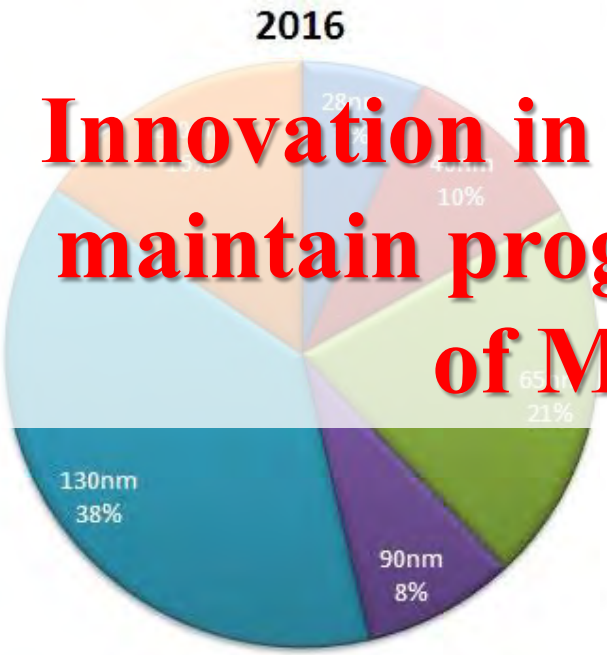

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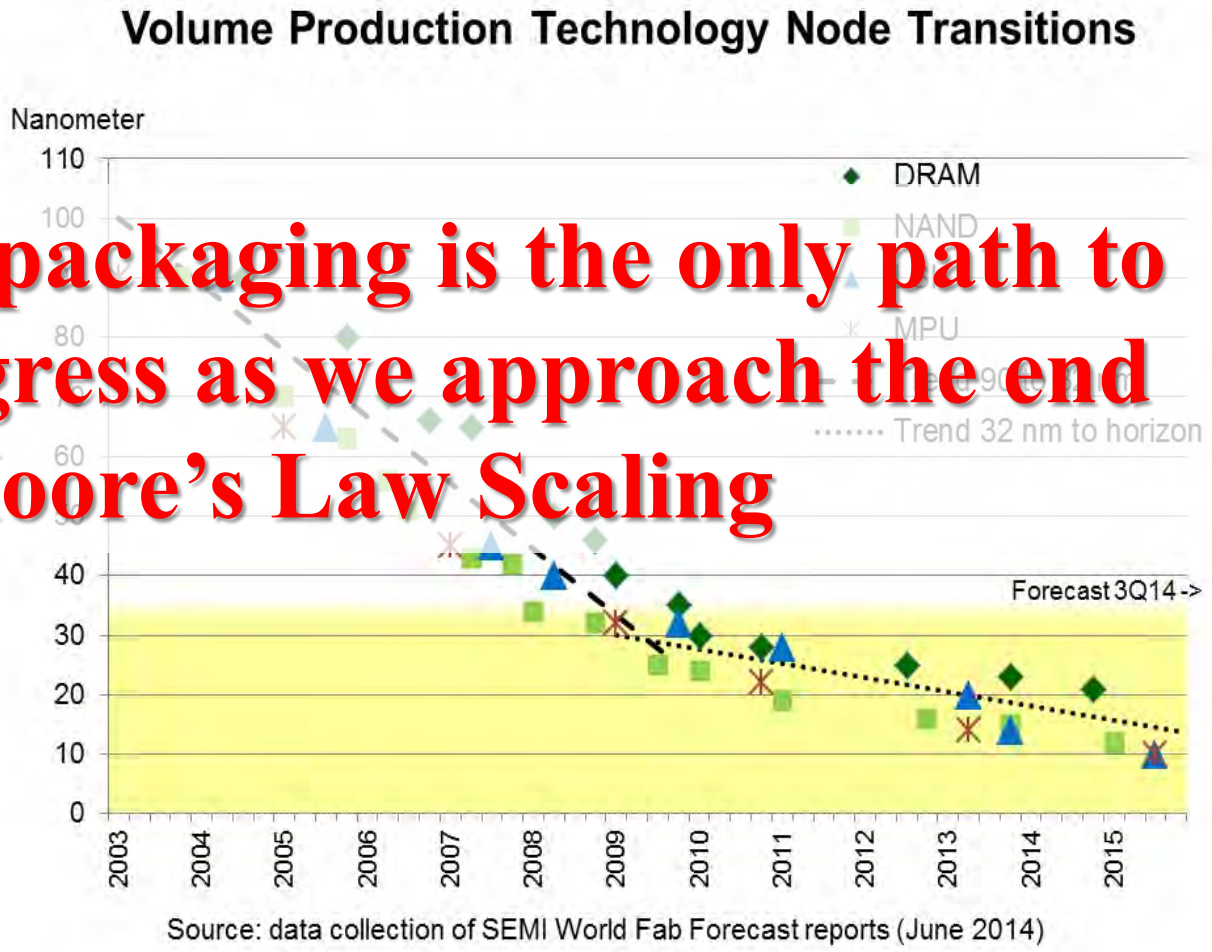
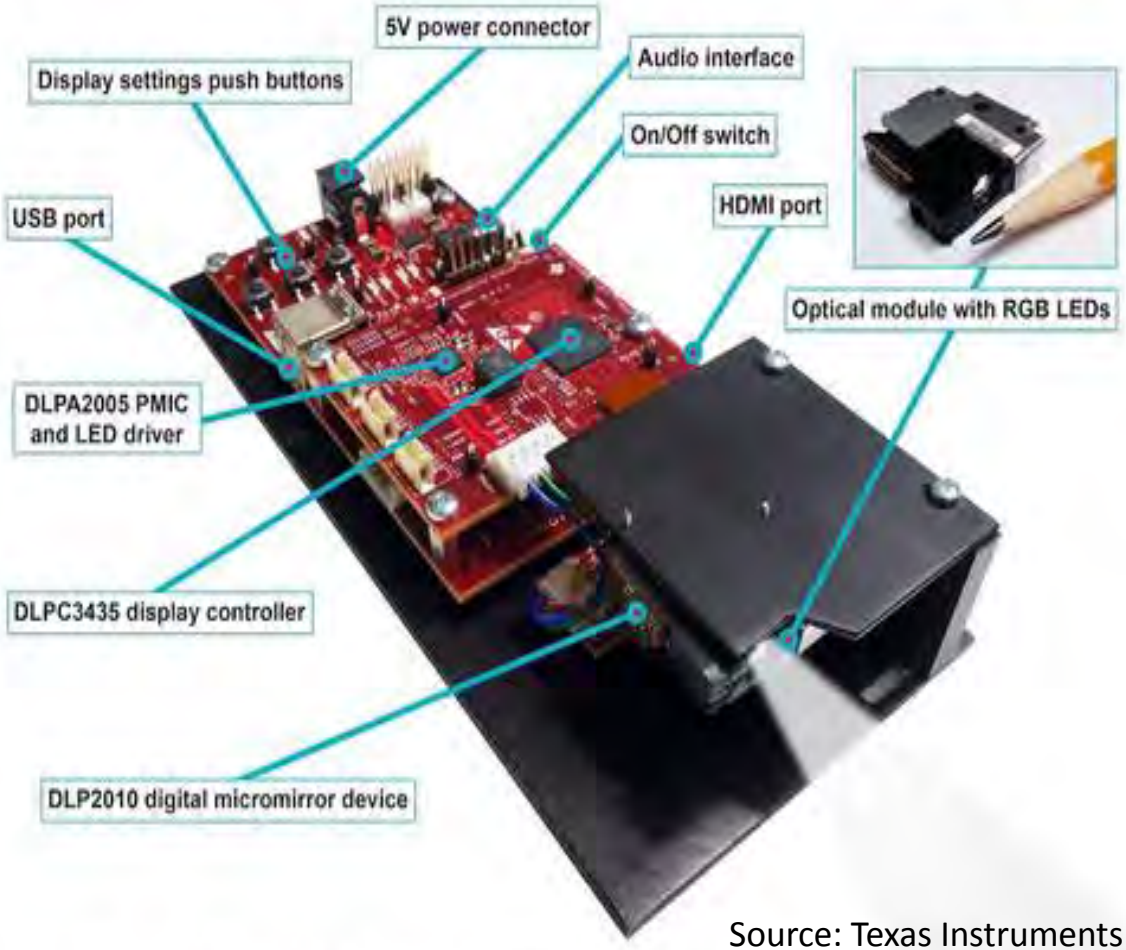


Innovation in packaging is the only path to maintain progress as we approach the end of Moore's Law Scaling

Heterogeneous Integration in Packaging MEMS and Electronics for IoT

TI's latest digital light projector (DLP) is small enough to mount on eyeglasses for a heads up display, or with one for each eye, for virtual reality It comes built into Samsung's Galaxy Beam 2



Source: Texas Instruments

DLP® LightCrafter™ Display 2010 evaluation module

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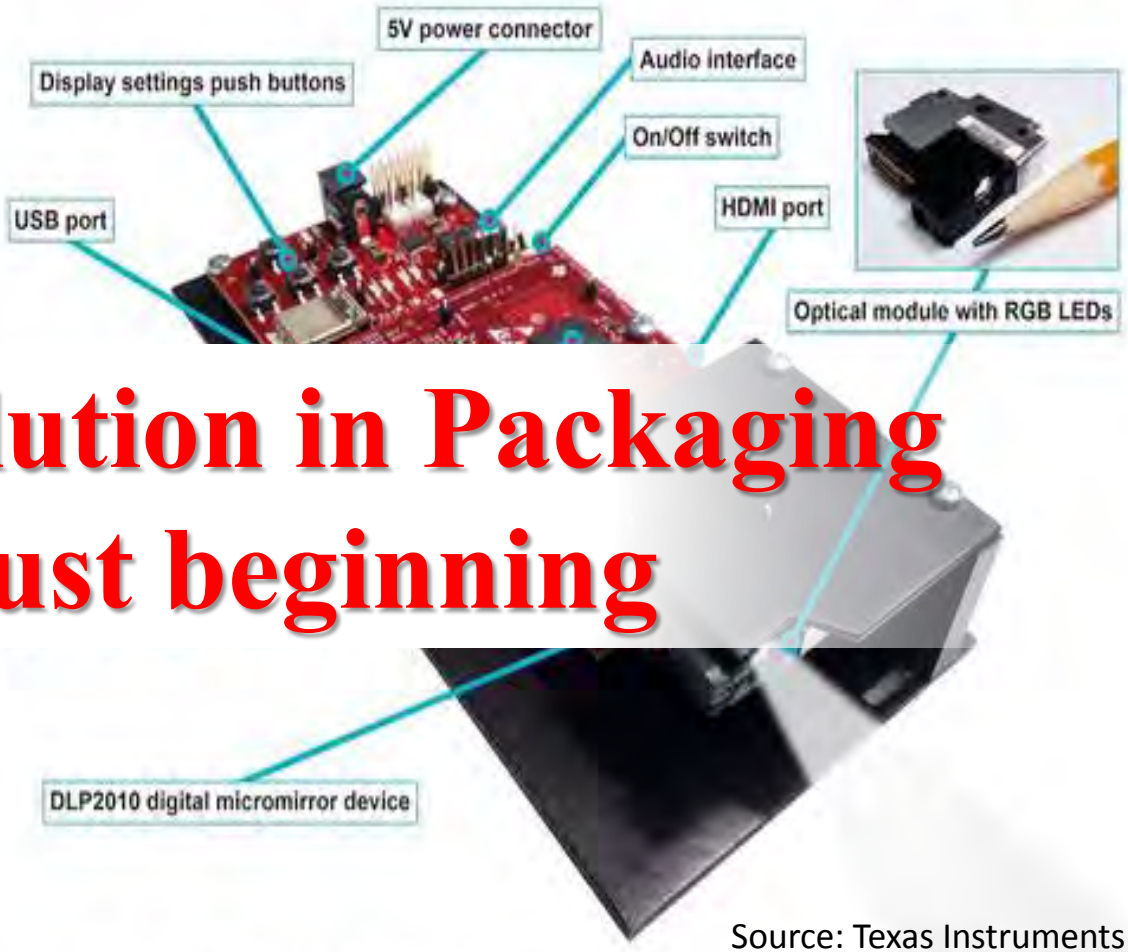


The Revolution in Packaging is just beginning

Source: Texas Instruments

DLP® LightCrafter™ Display 2010 evaluation module

Major Challenges

Power

Latency

Thermal management

Bandwidth density

Cost

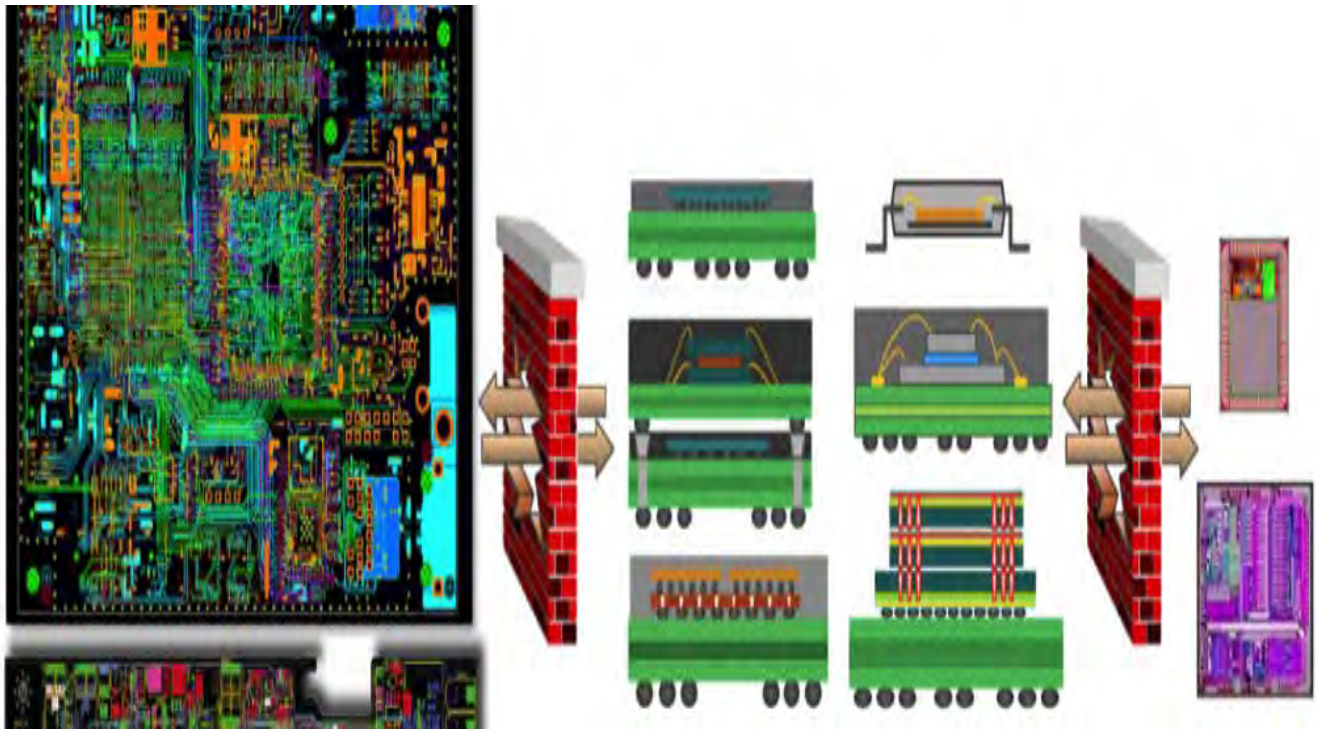
We must move things closer together

Co-design and Simulation Tools for Packaging are Critical Needs

Tools that integrate across the boundaries of device, package, printed circuit board and product will speed the process of migration to higher density (SoC, SiP, 2.5D, 3D, etc.).

This enables:

- ✓ Increased performance and bandwidth
- ✓ Decreasing latency, power, size, cost
- ✓ Reduced time to market



Reducing power requirements and ensuring reliability and power integrity at the point of use are major challenges.

What are the potential solutions?

How Can We Reduce Power?

- ✓ Continue Moore's Law Scaling
- ✓ Reduce leakage currents **(new transistor designs)**
  - Transistors are less than 10% of IC power today and going down
- ✓ Reduce on-chip Interconnect power by:
  - Improved conductor conductivity **(new material)**
  - Decrease capacitance **(new material)**
- ✓ Reduce interconnect length **(3D integration)**
- ✓ Reduce operating frequency **(increased parallelism)**
- ✓ Reduce operating voltage **(increased parallelism)**
  - Voltage regulator per core
- ✓ Reduce high speed electrical signal length
  - Move photons closer to the transistors **(On-package photonics)**

Thermal management is critical due to higher circuit density and lower operating temperature requirement.

What are the potential solutions?

Potential Thermal Management Solutions

- ✓ **Don’t make heat in the first place**
- ✓ **Improved thermal conductivity through new materials**
- ✓ **Incorporation of microfluidics, heat pipes**
- ✓ **Segregation of high temperature components**

Don't Make Heat in the 1st Place

IBM's Neurosynaptic Processor

- ✓ 5.4 billion transistors (biggest chip IBM ever made)
- ✓ 70 milliwatts power (20 milliwatts per cm^2)
  - 5,000 X cooler than todays MPU's
- ✓ Fully scalable
- ✓ End goal is a "brain in a box"
- ✓ 100 billion synapses at 1 KW
- ✓ Applications include
  - Smartphones
  - Other mobile devices
  - Cloud services with this technology.

IBM's neurosynaptic processor, 1 M Neurons and 256 M Synapses

"The chip delivers 46 billion SOPS per Watt -- literally a supercomputer the size of a postage stamp, with the weight of a feather and using a power source the size of a hearing aide battery,"

Dharmendra Modha, IBM fellow

Source: IBM

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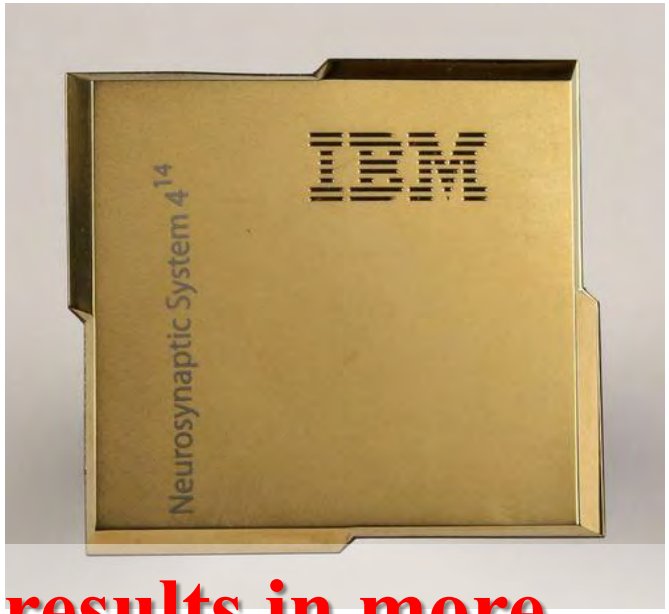

IBM's neurosynaptic processor, 1 M Neurons and 256 M Synapses

Increasing Power Efficiency results in more advantages than just thermal management

"The chip delivers 46 billion SOPS per Watt -- literally a supercomputer the size of a postage stamp, with the weight of a feather and using a power source the size of a hearing aide battery,"

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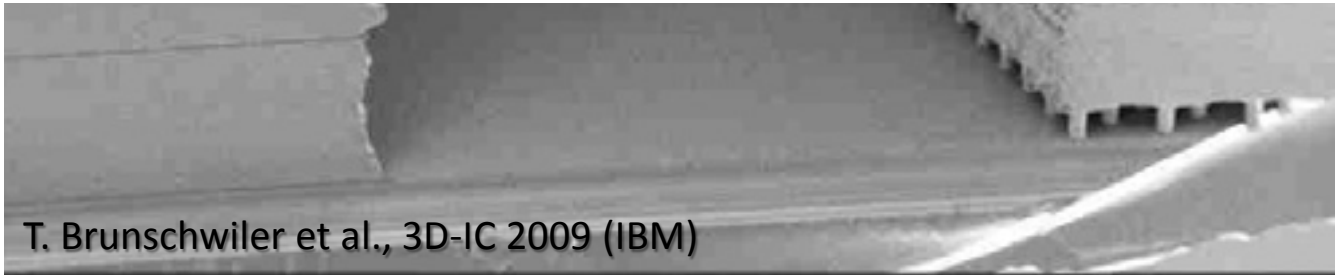
Microfluidic Cooling Is One Solution

It works but It is likely to remain too expensive for most applications



Physical density of Bandwidth is a roadblock.

Data processing in the cloud will be waiting for data much of the time with current bandwidth and latency limitations.

What are the solutions?

Potential Bandwidth/Latency Solutions

- ✓ **Put as much function into Photonics as possible**
- ✓ **Move photonics closer to the transistors**
- ✓ **Improve O to E conversion and modulation density through sub-wavelength confinement of photon energy**
- ✓ **Flatten the network architecture to minimize switches**
- ✓ **Increase bandwidth per fiber**

Several "Potential Solutions" impact more than one Category.

I will address each major multi category item under four topics:

- ✓ New Materials
- ✓ Photonics Close to Transistors
- ✓ Cost reduce Manufacturing
- ✓ Package Architecture

Conductors Are Changing

Composite Copper is in evaluation.

Current status:

Measurement	Conventional Copper	TeraCopper®
Resistivity (Ohm·cm)	1.66×10^{-6}	1.26×10^{-6}
Conductivity (S/m)	6.02×10^{7}	7.94×10^{7}
Increase in Conductivity	N/A	32%
Avg. Current Capacity(Amps/cm^2)	3.88×10^{4}	5.57×10^{4}
Increase in Current Capacity	N/A	44%

The first electrical performance improvement in copper since 1913 makes composite copper the most electrically conducting material known at room temperature.

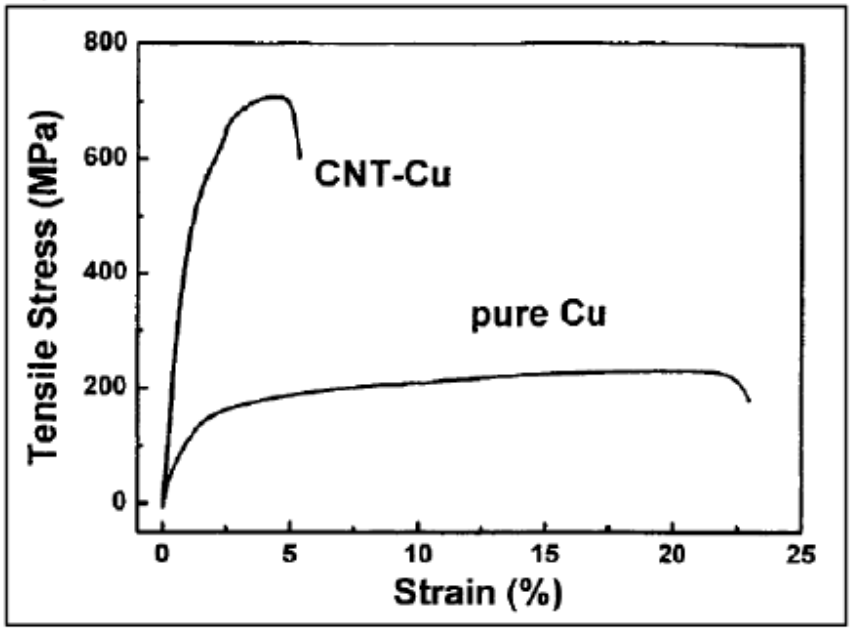
Targets for improvement compared to conventional copper are:

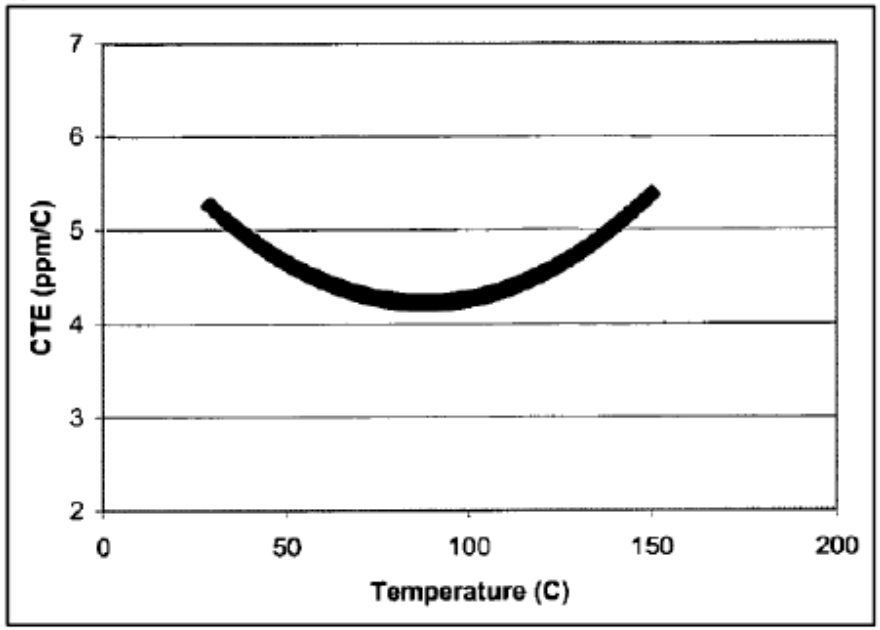
- ✓ **100 % increase in electrical conductivity**
- ✓ **100% increase in thermal conductivity**
- ✓ **300% increase in tensile strength**

Composite Cu Properties

Measured Properties show:

- ✓ The strength of the Cu-SWCNT composite is more than twice that of pure copper
- ✓ Ductility is significantly lower.
- ✓ Coefficient of thermal expansion ranges between 4 to 5.5x10-6/°C vs 17x10-6/°C for pure Cu.





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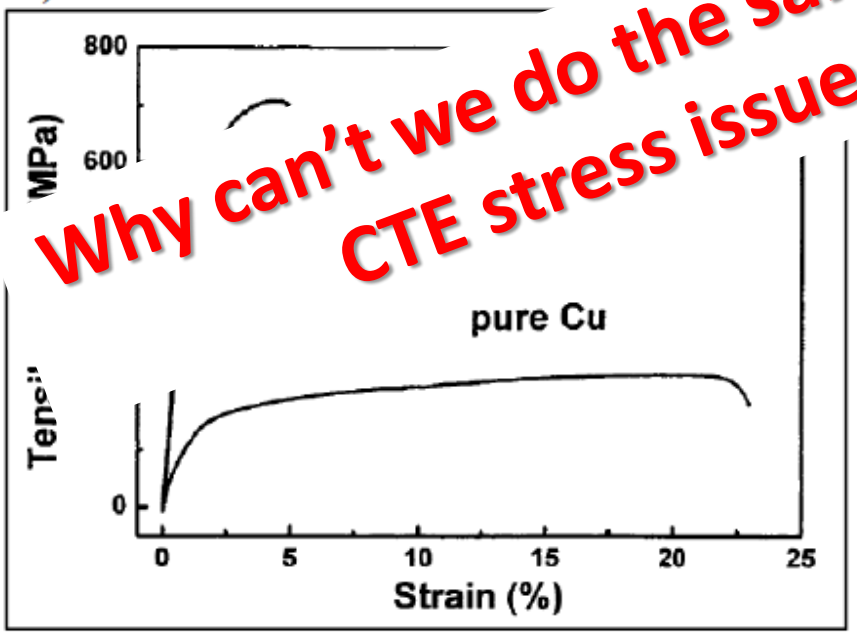
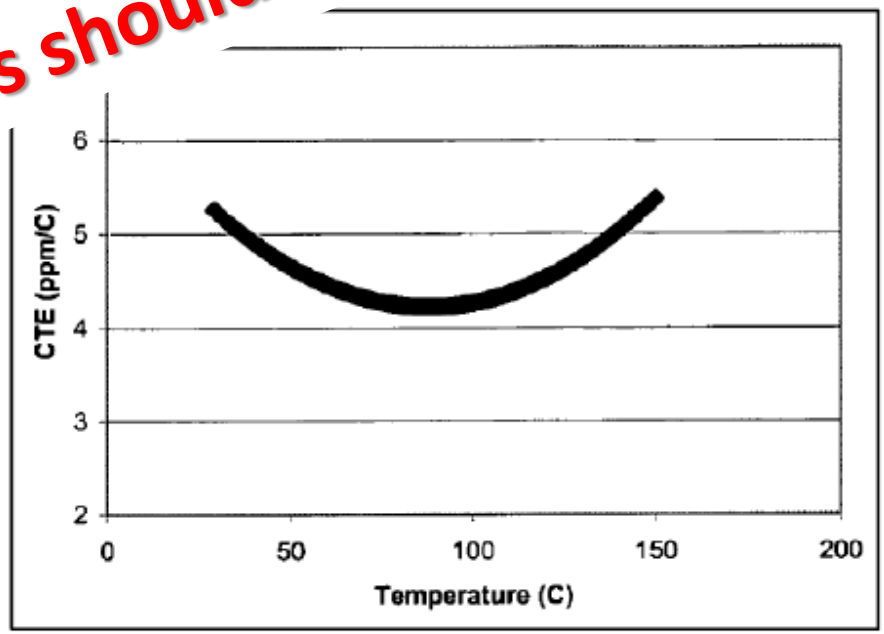
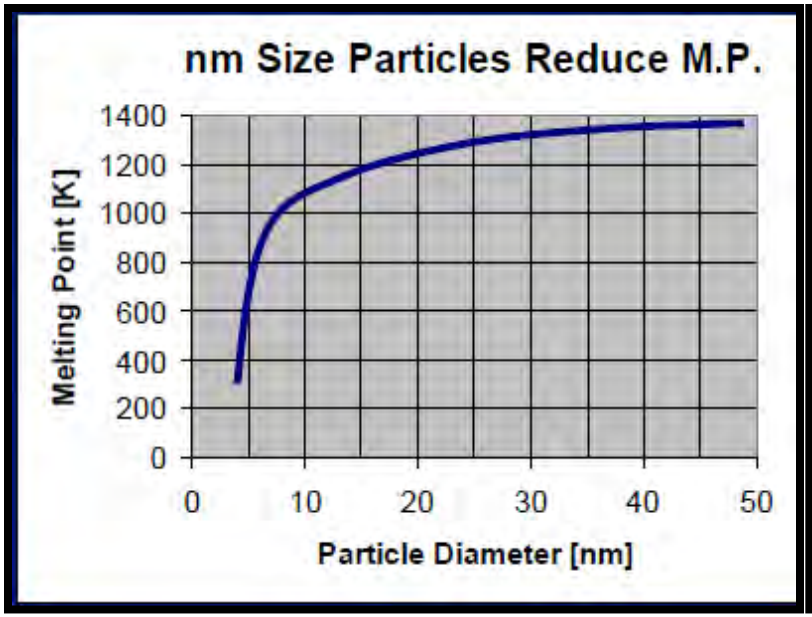
Why can't we do the same for package substrates? CTE stress issues should be solved!

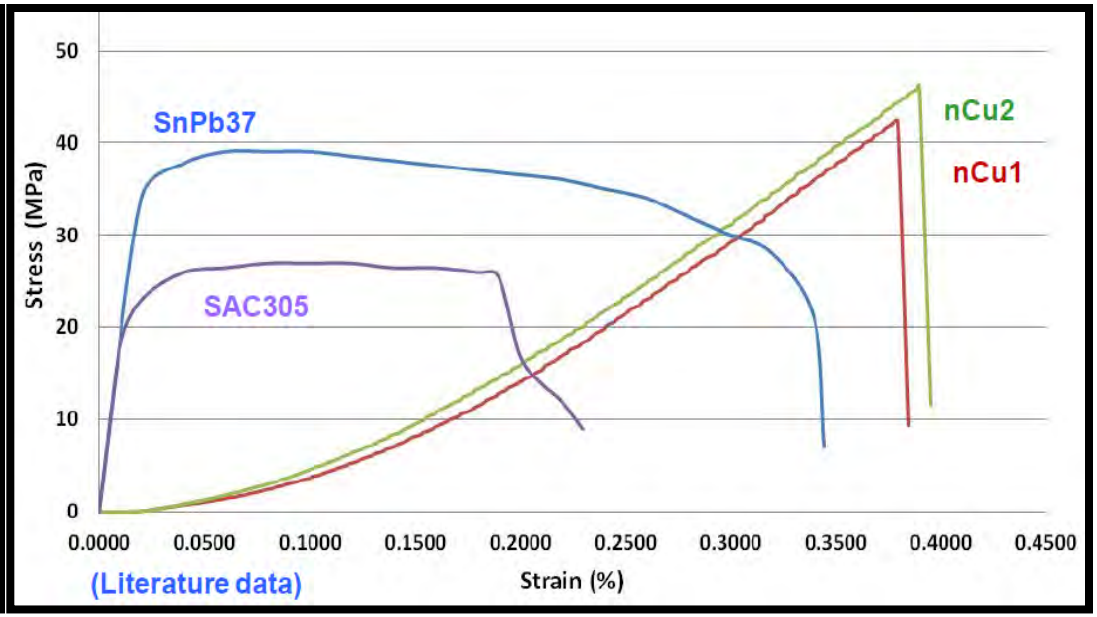




Low temp Cu Nano-solder

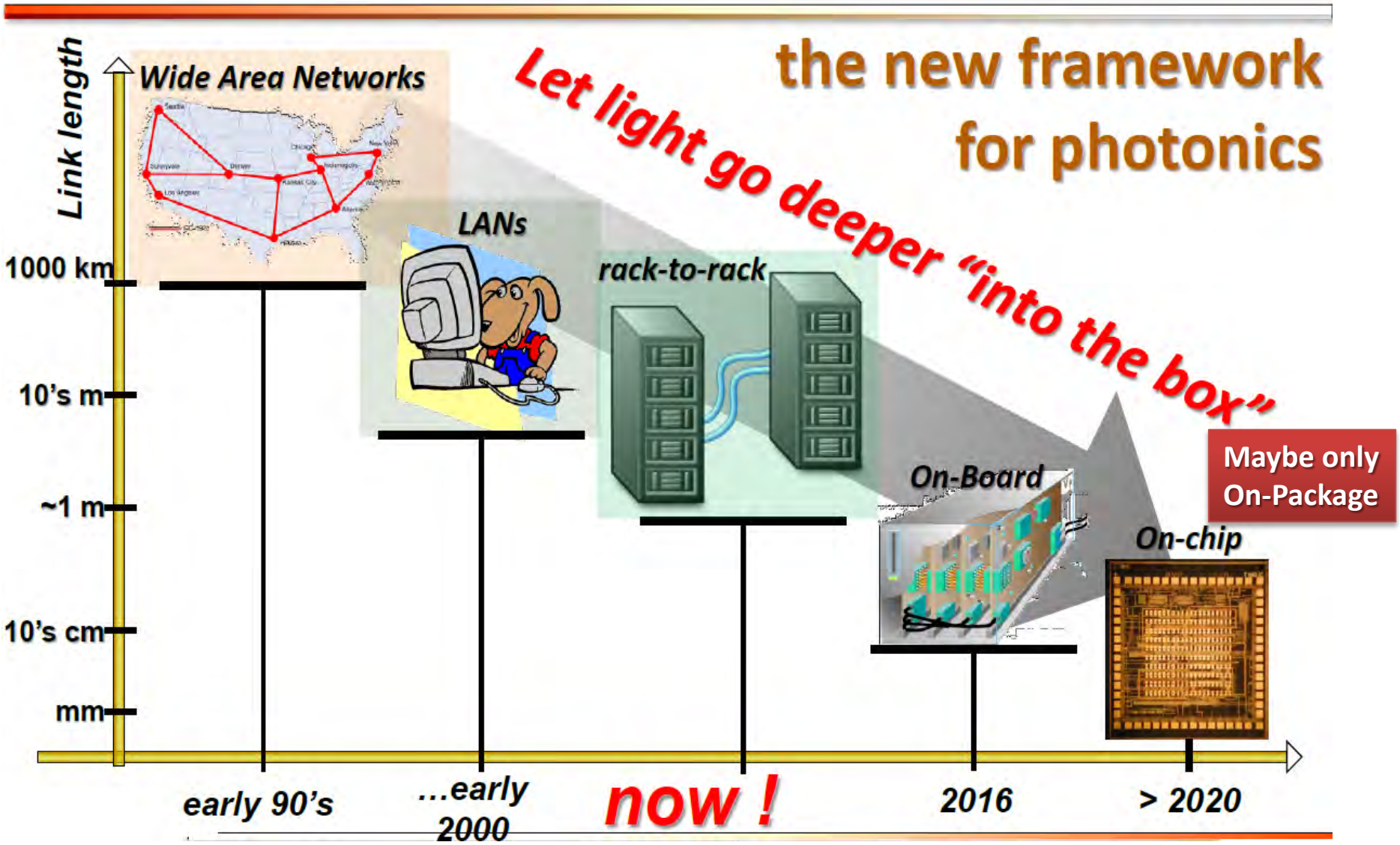
- ✓ **Package assembly at low temp (100C)**
- ✓ **Reflow solder to PCB <200C**
- ✓ **Consistent with Direct Interconnect Bonding**





Move Photons as Close as Possible to the Transistors

Photonics Penetration In The Network



Source: Dr. Nikos Pleros
Aristotle University

What Are The Challenges?

- ✓ **Silicon photonics connections are too expensive for on-chip and perhaps for on-package applications**

  Directed research can change this

- ✓ **Roadblocks:**
  - Co-design tools are not available
  - Size of optical components
  - Lowest power requires heterogeneous integration with new mechanical and thermal challenges
  - Thermal stability of key components requires temp control
  - Hot spots in SiP assemblies and on-chip.
- ✓ **Solutions will require research and development**
  - New materials will be a key
  - TSVs filled with polymer for waveguide?
    - It can also carry electrical signals in TSV lining.

…….and things we have not yet thought of!

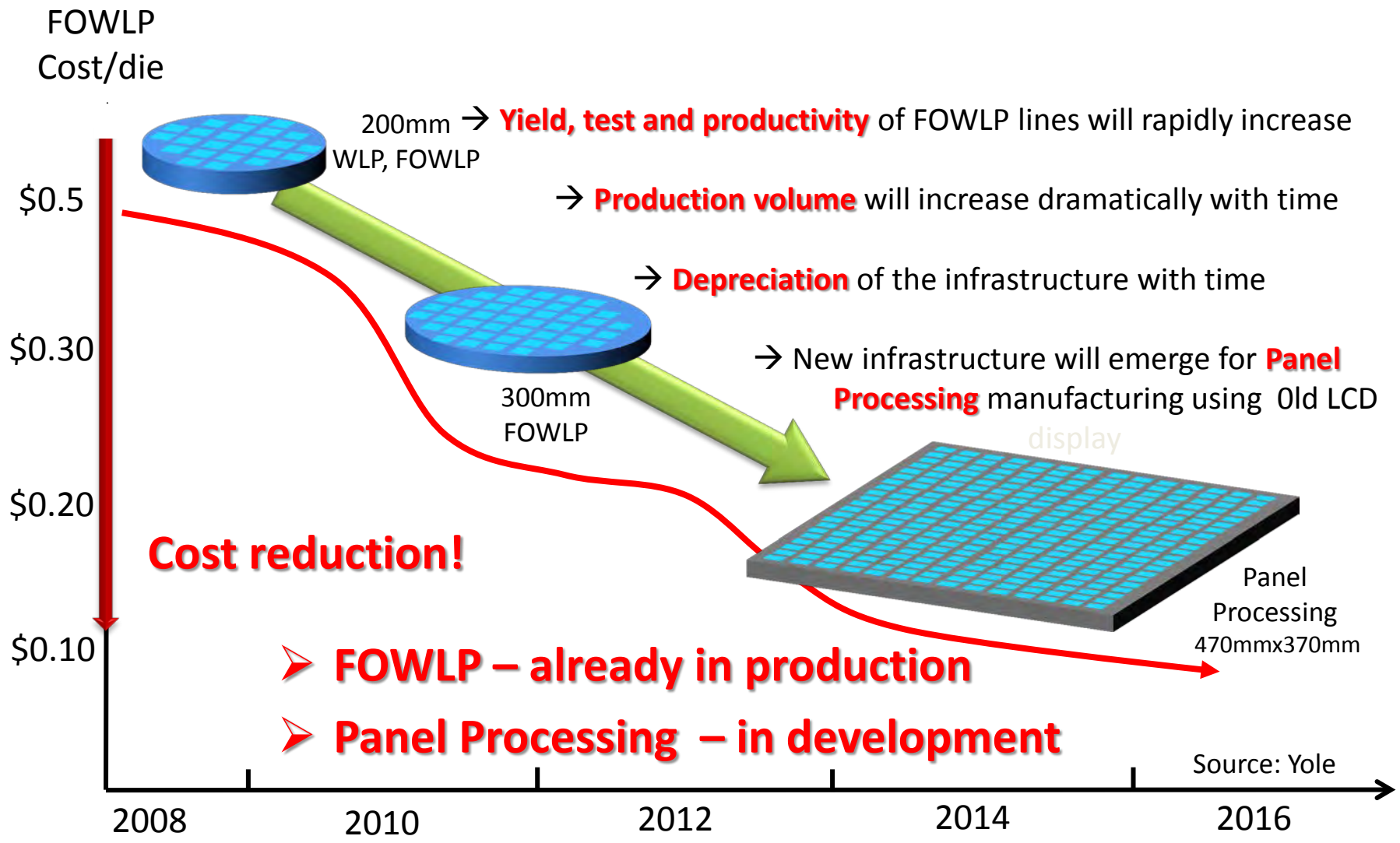
Co-Integration of Technologies

Use each technology where it is the best:

- ✓ Electronics
  - Active logic and memory (Processing and routing)
  - Smallest size
- ✓ Photonics
  - High bandwidth
  - Energy efficient
  - Long and intermediate distance
- ✓ Plasmonics (R. Zia et al., "Plasmonics: the next chip-scale technology", Materials Today 9(7-8), 2006)
  - Much smaller than photonic components
  - Potentially seamless interface between Optics and Electronics
  - Low power active functions

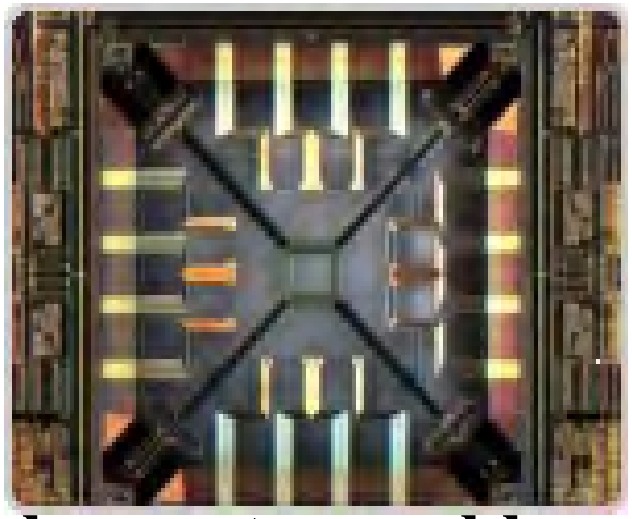
Cost Reduction in Manufacturing

WLP, FOWLP and Panel Processing Increase Parallelism and Reduce Cost



WLP for MEMS Devices

MEMSIC, a MEMS sensor company manufactures a 3 axis accelerometer utilizing WLP technology



Wafer Level Packaging of 3D accelerometer enables:

- ✓ 60 percent reduction in cost
- ✓ 50 percent reduction in size

A packaging solution enabling new generations of consumer devices (phones, tablets, toys and wearable devices)

Reduce Processing Steps

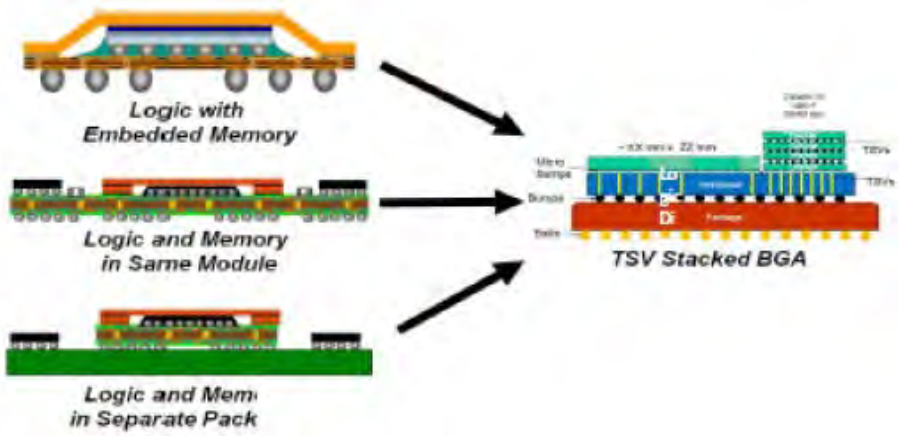
Remove package underfill

- ✓ New materials and lower processing temperature to reduce stress **Ziptronix DIB** **Cu nano-solder**
  - – Reduce CTE differential **Ultra-conducting CU**
- ✓ Lower modulus materials with improved fracture toughness **New ULK dielectrics**
- ✓ Improved interfacial adhesion **Alchimer metal**
- ✓ Reduce stress concentration by design **Simulation**

Packaging Architectures in use Today and In the IoT/Cloud Driven Future

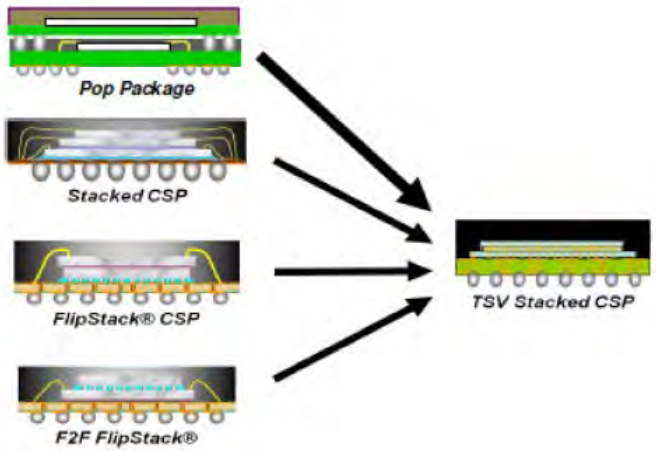
Advantages Of The 2.5D/3D Integration

2.5D Integration Improvement



- 100X improvement in die to die Bandwidth per watt
- Power reduced by 50%
- 5X latency reduction

3D-TSV Integration Further Improvement



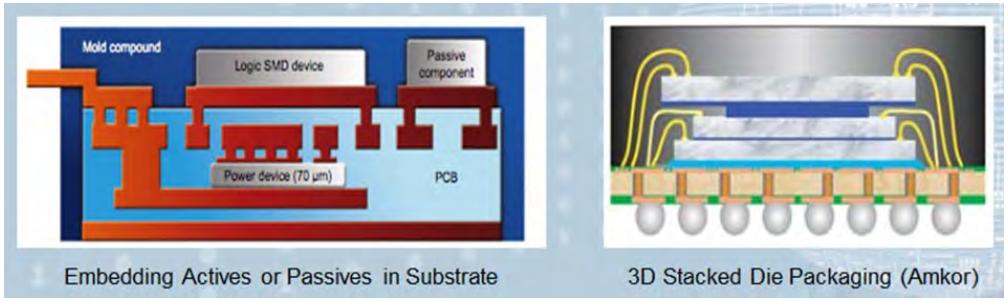
- 8X improvement in Bandwidth
- Power reduced by 50%
- Reduced thickness

Source: Amkor

3D Packaging is also for Power Devices
Particularly for SiP Components

3D Power Packaging Offers several advantages

- ✓ Reduced footprint
- ✓ Reduced volume
- ✓ Increased power density w/cm^2
- ✓ Incorporates embedded components



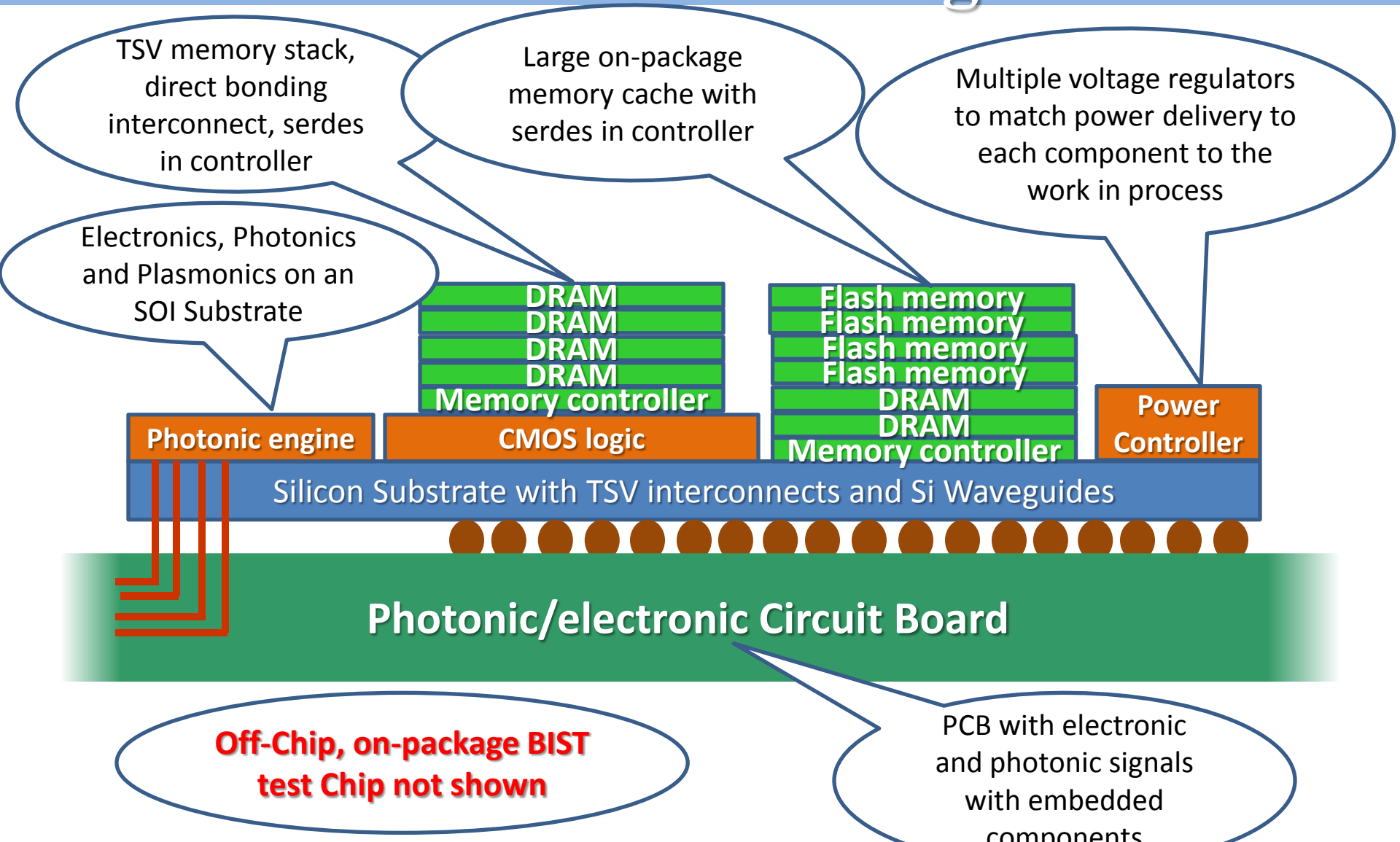
Applications driving the need for 3D power packaging

DCDC 3D Packaging Survey - Identified Important Markets

	0 - 10W	11 - 50W	50 - 250W	251 - 500W	501 - 999W	1KW+
Industrial	☆☆☆	☆☆☆	☆☆	☆	☆	☆
Military/Aero	☆☆☆	☆☆☆	☆☆	☆		☆☆☆
Smartphone/tablet	☆☆☆☆☆	☆	☆			
Server	☆☆☆☆	☆☆☆☆☆	☆☆☆☆☆	☆	☆	
PC	☆☆	☆☆☆☆	☆☆☆			
Comms	☆☆☆	☆☆☆☆☆	☆☆☆☆	☆		
Consumer	☆☆☆	☆☆☆	☆☆			
Transport/Auto	☆☆	☆☆	☆☆	☆☆		☆☆

SiP Components

A Potential Solution:
2.5D Photonic Co-integrated SiP



Summary

Requirements for IoT/Cloud driven Global Network

- ✓ **Cost and power reduced by >10^4**
- ✓ **Flatten the architecture increase ports by >10^6**
- ✓ **Reduce latency**
- ✓ **Support software defined networks**

Technology identified can deliver 10^3 improvement at most.

A majority of improvement we see comes from packaging.

Innovation is needed but is it practical to find another order of magnitude?

In the first 40 years of Moore's Law scaling every parameter improved by more than one million times.

Maybe 2 orders of magnitude in 15 years is too conservative

Thank You for Your Attention