IEEE Components, Packaging and Manufacturing Technology Society
Orange County Chapter

Friday, July 19, 2013

SIGNAL INTEGRITY FUNDAMENTALS ONE DAY SHORT COURSE

Instructors
Stephen Hall and Howard Heck
Intel Corporation

OVERVIEW:
This one-day short course provides practicing design engineers an in-depth introduction into the fundamentals of signal integrity. It covers the practical and theoretical aspects necessary to design modern high-speed digital systems at the chip, package, and board levels. Attendees will learn from Stephen Hall and Howard Heck, two leading experts from Intel Corporation.

WHO SHOULD ATTEND:
Engineers and engineering managers who need a detailed introduction to signal integrity, layout engineers who support high-speed design, and serial I/O buffer circuit designers.

TOPICS:

- High Frequency SI Challenges
- Transmission lines
- Skin effect, dielectric loss, and surface roughness
- Single-ended and differential signaling
- Cross-talk
- Eye diagram analysis
- High-speed serial interconnections
- Equalization and de-emphasis
- Jitter
- Simultaneous Switching Output noise (SSO)
- Power distribution

ABOUT THE INSTRUCTORS
Stephen Hall, began his career in 1992 in the Special Purpose Processor Division of the Mayo Foundation developing multi-gigabit modeling for X-band digital radar and serial optical links. In 1996, he joined Intel, as lead designer for buses on Pentium® II, III and IV, coordinated research with universities, led research teams in high-speed modeling and taught Signal Integrity courses. He published the textbook "High-Speed Digital System Design" in 2000 and co-authored "Advanced Signal Integrity for High-Speed Digital Designs" in 2009 with John Wiley & Sons. From 2003 to 2007, he researched new modeling and measurement for channel speeds up to 30 Gb/s and is currently investigating signal integrity associated with high performance small form factor computing devices. Stephen holds 25 patents (issued and pending) and has authored/co-authored 26 journal and conference papers.
Howard Heck: Since joining Intel in 1995, Howard held R&D engineering and management positions for system electrical technologies (interconnect, power, EMI). He led development for Pentium® II 100 MHz Host Bus, earning an Intel Achievement Award, and managed teams that defined and delivered technology for Direct RDRAM™, DDR II, Pentium® 4 Host Bus, and Accelerated Graphics Port (AGP) interfaces. Prior to DEG, he led Advanced Signaling Technologies in Intel's Systems Technology Lab, focusing on modeling, simulation, measurement, and technology for 10+ Gb/s signaling. He currently leads specifications and interconnect solutions for USB 3.0 technology. Howard earned the B.S.Ch.E. degree from Northwestern University in 1985, and the M.S.E.E. degree from the National Technological University in 1994. From 1985-1995 he was employed by IBM's PCB manufacturing and high performance packaging lab, where he led electrical development of HyperBGA™ packaging technology. Since 1997, Howard has served as Adjunct Professor at Oregon Graduate Institute, where he teaches High Speed Digital Interconnect Design. He has presented papers at several industry conferences, holds ten patents with twelve pending and is a Senior Member of the IEEE.

Date and time: **Friday, July 19th, 2013 7:45am – 5:10pm**

Location: **Calit2 Building, University of California – Irvine (Please see map on the next page)**

Registration Fee: **IEEE members - $30; Non-members of IEEE - $40; Students - $30**
(Prices will increase by $10 for non-student registrations on July 1, 2013)

Register online at http://www.eventbrite.com/event/5563921840#.

For questions on Registrations, please contact Raj Peddi at Raj.Peddi@us.henkel.com.

IEEE Components, Packaging and Manufacturing Technology Society
Orange County Chapter

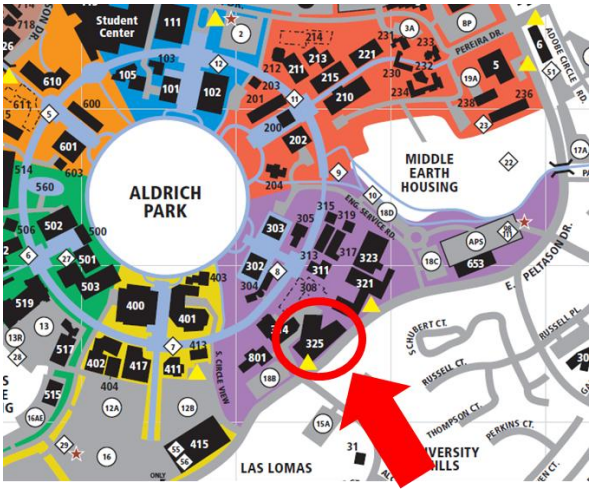
Friday, July 19, 2013 Tutorial

SIGNAL INTEGRITY FUNDAMENTALS ONE DAY SHORT COURSE

TENTATIVE AGENDA

Time	Topic
07:45 - 08:15	Registration Introductory remarks: Dr. Lawrence Williams, ANSYS
08:15 - 08:30	"The Future of Signal Integrity"
08:30 - 10:00	Causal Transmission Lines (S. Hall) 1. Classic t-line theory 2. Causal requirements 3. Physical dielectric models
10:00 - 10:15	Coffee Break (15 min)
10:15 - 11:45	Crosstalk & Differential Signaling (H. Heck) 1. Classic circuit model 2. Differential signaling 3. AC Common Mode
11:45 - 12:45	LUNCH (1hour)
12:45 - 02:45	Non-ideal Phenomena (S. Hall) 1. Non-ideal return paths and SSO 2. Vias (resonance & crosstalk) 3. Surface roughness 4. Environment
2:45 - 3:00	Coffee Break (15 min)
3:00 - 4:00	Signal Analysis Basics (S. Hall) 1. Eye diagrams 2. Peak Distortion Analysis
4:00 - 5:00	Equalization (H. Heck) 1. Equalization theory 2. De-emphasis
5:00 - 5:10	Closing Remarks

LOCATION & PARKING INSTRUCTIONS



There is a University fee of $7 for parking. Parking will be available in the Advanced Parking Structure (APS) off East Peltason Drive.

For more information please call any of the following officers of the IEEE CPMT OC Chapter: ***Follow us on LinkedIn.***

Raj Peddi (714) 368-2208 Larry Williams (714) 417-9311 x449 Tom Gregorich (949) 926-3939