Your Partner Throughout the Product Life Cycle
Who is DfR Solutions?

The Industry Leader in Quality-Reliability-Durability of Electronics

50 Fastest Growing Companies in the Electronics Industry
- Inc Magazine

Best Design Verification Tool
- Printed Circuit Design

2012 Global Technology Award Winner
10 Years of Providing Solutions to the Electronics Marketplace

- DfR / DfM / DfT / DfS..... DfX
- Finite Element / Fluid Dynamics
- Physics of Failure Modeling
- FMEA / FTA
- 3rd Party Design Review
- Failure Analysis
- Root Cause Investigations
- Forensic Engineering
- Circuit Analysis
- Connector/Wiring Selection
- Analog/Power Design
- Material Characterization
- PCB / PCBA Onsite Audits
- Pottings and Coatings
- Software Risk Mitigation

End-to-End Quality and Reliability Expertise
Technology Risk Evaluation: GaN FETs

- Identified current state of technology and potential risks
  - Difficulty in manufacturing
  - Limited supply of reliability data
  - Recommended **four condition testing** scheme for qualification

**Schottky contact:** normally stable at 300°C, no gate sinking effect of DC bias

**Charge trapping:** effect of cap, passivation, surface preparation

**Ohmic:** thermal degradation observed at \( T_j > 300°C \)

**Hot electron-induced trap generation**
+ Trapping at deep levels

**Piezoelectric-induced strain and relaxation trap generation**
+ Trapping at deep levels
Market Benchmarking: SOC Power Conversion Devices

- Performed comprehensive benchmarking of customer solution and market competitors

- Captured case temperature rise and efficiency under multiple voltages, power loads, and ambient temperatures
  - This level of assessment was not previously performed; provided key insight into derating recommendations and margining
Component manufacturer pushing the limits to increase market share
- Driving RF CMOS transistors beyond foundry’s specification
- New packaging technologies (copper pillar, copper wirebond, low Tg underfill)

Comprehensive assessment
- Initial transistor life prediction
- Finite modeling for prediction of 1st and 2nd level lifetime
- Guidance on qualification plan
IC Lifetime Prediction Methodology

- Models the simultaneous degradation behaviors of multiple failure mechanisms on integrated circuit devices
- Devised from published research literature, technological publications, and accepted degradation models from:
  - NASA/JPL
  - University of Maryland
  - Semiconductor Reliability Community
Customer Management: Application Notes

- Turnkey solution for application note development
  - Design recommendations (stencil, bond pad, solder mask)
  - Process optimization (reflow, wave, rework)

- Created defect identification guide
  - Cause of misalignment/voiding
  - Images of starved, bulbous solder joints
  - Troubleshooting guide

- Qualified to JEDEC and AEC
  - Range of environmental test conditions
Testing: Board Level Reliability (BLR)

Test Environments
- Temperature
- Temperature Cycling
- Temperature/Humidity
- Vibration
- Mechanical Shock
- Drop
- Bending
- Pull/Shear
- Combined Environment (Vibration + Temperature)

Test Methods
- JESD22 (A and B)
- AEC Q100
- IPC 97XX

Failure Analysis
- Decapsulation (gold and copper wire)
- Cross-Sectioning
- Optical and Electron Microscopy
Simulation: Modeling Warpage and BLR
Results: Over 1000 Satisfied Customers
Flip Chip Reliability Issues

Solder Bump vs. Copper Pillar
Flip Chip: Growing, but Not Dominant

Wire Bond vs Flip Chip Market

Interesting Fact: Did you know there is, practically, only one manufacturer of wire bond equipment?

Figure 6 – Total Package Cost Comparison
…but is Evolving

Flip-Chip bumping wafer forecast*
Breakdown by bumping metallurgy (12”eq wafers)

- Cu Pillar
- Lead Free Solder
- Sn/Pb Eutectic Solder
- Gold Stud + Plated

*3D micro-bumping included

(Yole Développement, February 2013)

Note: Yole forecasts can be inaccurate
Flip Chip SnAg Bump

- Silicon
- ELK Active layer
- USG protective Layer
- Underfill
- Soldermask
- Substrate
- Al Pad
- Pad Passivation
- PI/PBO Passivation
- Solder
- UBM
- Copper Pad
Flip Chip Copper Pillar

- Silicon
- ELK Active layer
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- Pad Passivation
- PI/PBO Passivation
- Underfill
- Solder
- Soldermask
- Copper Pad
- Substrate
- UBM
Copper Pillar History

- Copper pillar was first patented by IBM in 2001
  - Metal post solder chip connection (MPS-C2)

- In 2005, copper pillar interconnects placed in RF power amplifiers and front-end modules
  - Improved electrical stability and thermal performance
  - Elimination of through-GaAs vias, wafer thinning, and backside metallization

- Intel uses a combination copper pillar/SnPb joint for its 65nm Yonah and Pressler processors (2006)
The benefits listed by Intel
- Improved electromigration resistance
- Improved thermal conductivity
- Simplified underbump metallization
- Higher I/O density

Many believe the migration to copper pillar allowed Intel to avoid the low-Tg underfill fiasco
- These devices maintained high Tg underfill

Note, no mention of improved thermal cycling performance
Why Copper Pillar?

- One Word: Smaller Pitch
- Solder bumps are problematic below 125 micron pitch
  - Challenging to manufacture and assemble
- Drivers for smaller pitch
  - Needed for latest process nodes (28nm and below)
  - Allows for smaller devices (demand of mobile OEMs)
  - Reduces # of substrate layers (lower cost)
Flip Chip: A Balancing Act

- Flip Chip interconnections require a fine balancing act between die, interconnect, underfill, substrate/leadframe, and lid to avoid the ‘SEVEN’

  - Low-K Dielectric Cracking
    - During chip attach – White Bump
    - During underfill
  - Flip chip bump reliability
    - Solder fatigue of C4 SnAg bump
    - Temp cycling
  - Solder joint reliability
    - Solder fatigue of 2\textsuperscript{nd} level connection
    - Temp cycling
  - Warpage
    - Coplanarity of the package
    - Measured at (-55)°C and 260°C
  - Die backside stress
    - During chip attach
    - Die cracking
  - Bond line thickness
    - TIM thickness at various temps
    - Affects $\theta_{jc}$ (thermal resistance: Junction to case)
  - Electromigration
Solder Bump vs. Copper Pillar

- Is Copper Pillar more/less reliable than Solder Bump?
  - Answer: Depends!
  - Why?: Multiple flavors of flip chip devices and 1st level interconnections
Flavors of Flip Chip: Bare Die with Underfill

- Die
- Underfill
- Substrate
- Pads
- BGA ball
- PCB
Flavors of Flip Chip: Lidded

- Street
- Lid Adhesive
- Die
- Lid
- TIM
- Underfill
- Lid Foot
- Pads
- BGA ball
- Substrate
- PCB
Flavors of Flip Chip: Exposed Die + Molded + UF

- Street
- Die
- Underfill
- Mold
- Substrate
- Pads
- BGA ball
- PCB
Flavors of Flip Chip: Exposed Die + Molded
Flavors of Flip Chip: Overmolded
Which Copper Pillar?
Which Copper Pillar (cont.)

- Intel (above), Amkor (top right), and ASE (bottom right)

105 micron diameter pillar
Clear differences in regards to:
- Pillar dimensions (height and diameter)
- Pillar shape (square vs. oval vs. round)
- Pillar wall (tapered vs. straight)
- Ratio of pillar height to solder thickness
- Ratio of pillar diameter to UBM diameter
- Ratio of pillar diameter to bond pad diameter
- Presence/absence of compliance layer (polyimide)

These differences complicate an attempt to compare solder bump to copper pillar (or even copper pillars to each other).
Which Assembly Process?

- **Standard reflow process (solder paste)**
- **Modified reflow process (flux dip)**
- **Thermo-compression bonding**
  - Increasingly the dominant assembly process

*Thermo-compression (TC) Bonding with Non-Conductive Paste (NCP)*

*Figure 7. Process flow for thermo-compression bonding with non-conductive paste (TC+NCP) and resultant copper pillar bond.*
Thermocompression Bonding

- If the pitch gets fine enough, process moves to thermocompression bonding with non-conductive paste
  - Typically below 60 micron pitch
  - Actual thermocompression takes only 2 to 3 seconds (similar to wirebonding!)

- However, this results in a change in material properties of the underfill
  - The non-conductive paste (NCP) becomes the underfill
  - Typically, different material properties than standard underfill (lower Tg, lower modulus)

- Underfill properties will tend to dominate thermo-mechanical fatigue performance
Electromigration (EM) Reliability

- At similar dimensions, copper pillar outperforms solder bump in regards to electromigration (as much as 3X increase in lifetime\(^1\))

- Higher electrical and thermal conductivities reduce current density and temperature (primary drivers of electromigration)
  - Current crowding in solder bumps is highest at the entrance of the metal trace to the bump\(^2\)

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1. SPI, Cu Pillar and BOT Flip Chip, 2014
2. Y. Wang, Reliability of Cu Pillar Bumps for Flip Chip Packages
### Amkor EM Test Results (A. Syed, EPTC 2010)

<table>
<thead>
<tr>
<th>Bump Configuration</th>
<th>Stress Current (mA)</th>
<th>Temperature (deg C)</th>
<th># Samples</th>
<th># Failed</th>
<th>Test Hours Completed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cu Pillar</td>
<td>400</td>
<td>150</td>
<td>8</td>
<td>0</td>
<td>6300</td>
</tr>
<tr>
<td>Cu Pillar</td>
<td>550</td>
<td>150</td>
<td>8</td>
<td>0*</td>
<td>6300</td>
</tr>
<tr>
<td>Cu Pillar</td>
<td>700</td>
<td>135</td>
<td>10</td>
<td>0*</td>
<td>5300</td>
</tr>
<tr>
<td>Cu Pillar</td>
<td>700</td>
<td>150</td>
<td>8</td>
<td>0*</td>
<td>6300</td>
</tr>
<tr>
<td>SnAg</td>
<td>400</td>
<td>135</td>
<td>7</td>
<td>1</td>
<td>5300</td>
</tr>
<tr>
<td>SnAg</td>
<td>400</td>
<td>150</td>
<td>8</td>
<td>2</td>
<td>6300</td>
</tr>
<tr>
<td>SnAg</td>
<td>700</td>
<td>135</td>
<td>7</td>
<td>2</td>
<td>5300</td>
</tr>
<tr>
<td>SnAg</td>
<td>700</td>
<td>150</td>
<td>8</td>
<td>8</td>
<td>4050</td>
</tr>
<tr>
<td>Eut Sn Pb</td>
<td>400</td>
<td>135</td>
<td>8</td>
<td>2</td>
<td>5300</td>
</tr>
<tr>
<td>Eut Sn Pb</td>
<td>400</td>
<td>150</td>
<td>8</td>
<td>8</td>
<td>2167</td>
</tr>
<tr>
<td>Eut Sn Pb</td>
<td>700</td>
<td>135</td>
<td>8</td>
<td>8</td>
<td>1992</td>
</tr>
<tr>
<td>Eut Sn Pb</td>
<td>700</td>
<td>150</td>
<td>8</td>
<td>8</td>
<td>1240</td>
</tr>
<tr>
<td>High Pb</td>
<td>400</td>
<td>135</td>
<td>8</td>
<td>6</td>
<td>5300</td>
</tr>
<tr>
<td>High Pb</td>
<td>400</td>
<td>150</td>
<td>8</td>
<td>8</td>
<td>2200</td>
</tr>
<tr>
<td>High Pb</td>
<td>550</td>
<td>135</td>
<td>7</td>
<td>7</td>
<td>2267</td>
</tr>
<tr>
<td>High Pb</td>
<td>700</td>
<td>135</td>
<td>8</td>
<td>7</td>
<td>3550</td>
</tr>
<tr>
<td>High Pb</td>
<td>700</td>
<td>150</td>
<td>8</td>
<td>8</td>
<td>799</td>
</tr>
</tbody>
</table>
Electromigration (EM) Reliability (cont.)

- However, the switch from solder bumps to copper pillar will not result in similar dimensions
  - Solder bump: 80 to 100 micron diameter
  - Copper pillar: 25 to 60 micron diameter

- The ratio of interconnect (bump or pillar) diameter to UBM diameter will likely decrease to reduce stress on low-K dielectric

- Use of bump on trace (BOT) could also introduce areas of elevated current density
There is surprisingly little good test data on the relative performance of solder bump vs. copper pillar. Comparisons have primarily been through simulation.

Regardless of the interconnect technology (bump vs. pillar), underfill properties will dominate thermal cycling performance.

If the underfill needs to change, to NCP / NCF / molded underfill, this will tend to have a far greater effect than interconnect parameters.
Thermal Cycling Reliability (cont.)

- As a general statement, thermal cycling performance would be expected to be better

- Copper pillars can offer a larger standoff for a given pitch (more compliance in the interconnect)

- Larger ratio of copper to solder increases amount of intermetallic within the solder volume
  - Improves creep resistance (this why SAC405 is better than SAC305 which is better than SAC205, etc.)
### Intermetallics in Copper Pillar Interconnections

<table>
<thead>
<tr>
<th>No. of Temp. Cycle</th>
<th>1st layer Cu &amp; Sn (%)</th>
<th>2nd layer Cu &amp; Sn (%)</th>
<th>Sn (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 Cycles</td>
<td>9.7</td>
<td>37.3</td>
<td>53.0</td>
</tr>
<tr>
<td>300 Cycles</td>
<td>13.3</td>
<td>36.3</td>
<td>50.4</td>
</tr>
<tr>
<td>500 Cycles</td>
<td>14.6</td>
<td>47.9</td>
<td>37.5</td>
</tr>
<tr>
<td>700 Cycles</td>
<td>15.4</td>
<td>43.3</td>
<td>41.3</td>
</tr>
<tr>
<td>1000 Cycles</td>
<td>14.3</td>
<td>58.2</td>
<td>27.5</td>
</tr>
<tr>
<td>1500 Cycles</td>
<td>14.0</td>
<td>47.7</td>
<td>38.3</td>
</tr>
</tbody>
</table>

Note: Thickness of material in percentage (%) base.

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![Intermetallics in Copper Pillar Interconnections](image)

L. Kwang and T.K. Hwee, Flip Chip on Leadframe Assembly Using copper pillar bump technology

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![Intermetallics in Copper Pillar Interconnections](image)

J. Vardaman, Emerging Trends in Flip chip
Thermal Cycling Reliability (Simulations)

- Different papers have indicated different trends
  - Some claim lower stress (improved performance)
  - Some claim higher inelastic strain energy density (worse performance)

*Figure 4 Comparison of LF, Cu column bump w/ solder cap and Cu column bump w/o solder cap fcFBGA devices*

Y Wang, Reliability of Cu Pillar Bumps for Flip Chip Packages

M. Hseih, IEEE IMPACT, 2012
Change in Underfill (Decrease in Tg)

- Near the Tg, CTE changes more rapidly than modulus
- Large increase in the expansion with negligible change in the modulus can result in significant solder tensile stresses
Rise in Tensile Stress

High stresses generated in the solder due to CTE increase before modulus decrease.

\[ F = \frac{\Delta T (\alpha_2 - \alpha_1)}{\left( \frac{1}{A_1 E_1} + \frac{1}{A_2 E_2} \right)} \]
Effect of Mean Tensile Stress

- As mean tensile stress increases, fatigue lifetime drops due to diminished recovery of accumulated damage.

- Example: stress-controlled fatigue at 42 MPa amplitude
  - $\sigma_{\text{mean}} = 0$ MPa: lifetimes of 15K to 35K cycles
  - $\sigma_{\text{mean}} = 7$ MPa: lifetimes of 100 to 1K cycles

- For mean compressive stress or strain, recovery processes dominate; fatigue life is effectively infinite.

- At comparable stress amplitudes, lifetime in tension is up to 100X less than that in shear.
Temperature transitions through the critical temperature range decreases the life by an order of magnitude.
Consistency of solder between the copper pillar and bond pad also becomes critical.

Wetting along the sides of the copper pillar can result in very small bondline.

Insufficient coplanarity of the copper pillar can also result in joints with non-optimum geometry.
  - Copper plating process can result in pillar heights varying by as much as 25% (40 to 50 microns).
Discussions on reliability can be complicated by shift in failure site

Some studies have identified cracking in low-k dielectric after temperature cycling / thermal shock

The singular environmental may not detect these type of failure modes

R. Katkar et. al., Reliability of Cu Pillar on Substrate, 2011
ELK Cracking

- ELK cracking is often viewed as the biggest risk in regards to transition to copper pillar
  - Primarily occurs during flip chip bonding process
  - Some observation of cracking during underfill cure (during cool down)

- Key issues are to identify mitigation techniques
ELK Cracking Mitigation

- Tall copper pillars help decouple the interaction between the copper pillar and the low-K/ultra-low K/extreme low-K (ELK) dielectric
  - However, tall copper pillar is a tradeoff. Requires more plating time, decreasing through-put

- Larger ELK thickness

- Larger diameter

- Small attach at top or bottom

- Use of polyimide

M.C. Hsieh, IEEE IMPACT, 2012
ELK Crack Migitation (Large Diameter)

- Comparison of 80um (small) vs. 100um (large) diameter copper pillar
  - Copper pillar height of 50um and solder height of 20um

*Y Wang, Reliability of Cu Pillar Bumps for Flip Chip Packages*
ELK Crack Mitigation (Small Attach)

- Can increase compliance of the overall structure
- Used for bump on trace (BOT) geometry
  - SPIL recommends die bond pad ratio to trace width ratio not exceed 2X
PI Passivation

- The PI layer is softer:
  - Reduces stress
- Pad-Bump interface diameter is reduced to the PI passivation opening
  - The copper pillar height remains the same
  - The distance between the copper pillar corner to the pad passivation is increased
- Adding the PI layer:
  - Either at the die vendor or before bumping
Conclusion

- Copper pillar is increasing in popularity

- As each OSAT (and potentially foundry) has different technology and process, variations to improve reliability can be challenging
  - Especially considering die constraints

- Do not always rely on test!
  - Test conditions may not accurately convey to field environments