

Wafer Bonding Enables New Technologies and Applications

Teikoku Taping Systems

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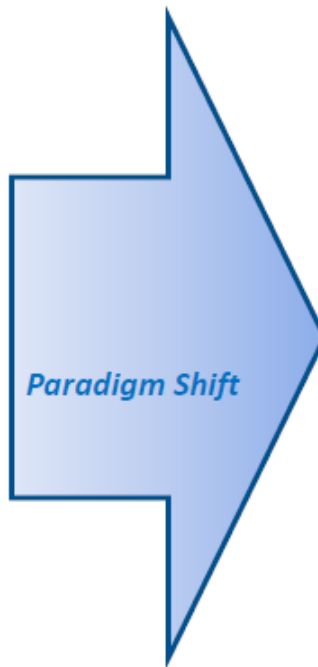
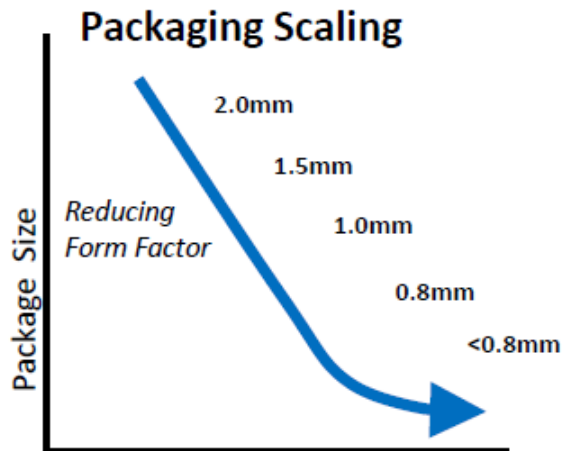
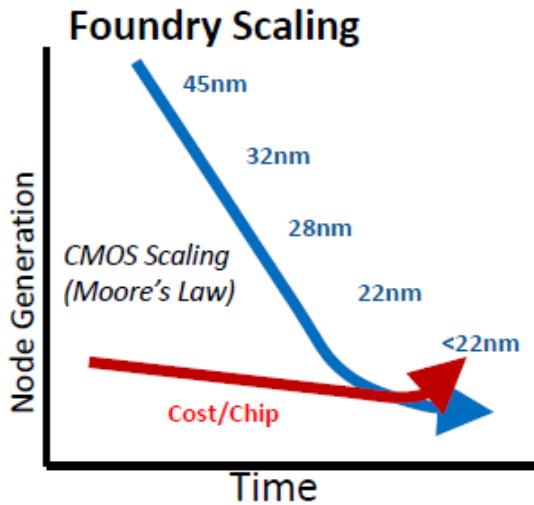
Prepared by: **Mark Franklin**



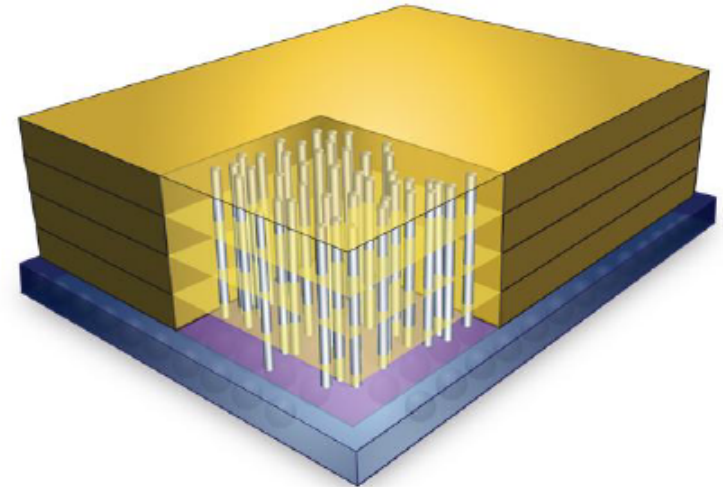
At a Glance

Forecasts for the demise of Moore's Law are fairly common. There is a limit to making smaller features where cost and complexity issues become prohibitive. The semiconductor industry has established, rather quickly, a new path forward focused around 3D stacking of integrated circuits. Adding a third dimension to an integrated circuit packs more transistors into the same small footprint without the need to shrink the features of the circuit. The layers are stacked like floors in a skyscraper effectively allowing Moore's law to continue, albeit, down a slightly different path. 3D integration or vertically stacked chips or wafers requires new technology and new equipment. Just as chemical mechanical polishing (CMP) became the enabling technology for the industry years ago; wafer bonding has been identified as its next enabling technology.

Changing Landscape



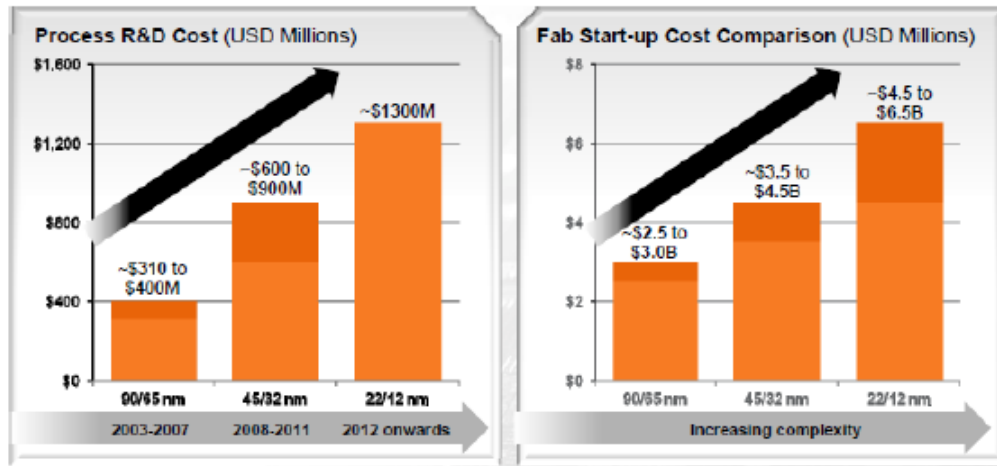
TSV-based 3D-IC Packaging



Critical performance metrics are shifting from CMOS Scaling and Package Form Factor to SYSTEM LEVEL Power Consumption and Bandwidth.

- Lack of cost effective lithographic solution is slowing down raw scaling.
- Parallel processing addresses issues of raw scaling – drive towards multi-core processors.
- Multi-core processors are limited by the memory wall.
- 3DIC will enable multi-core processors to break through the memory wall – Stacking of memory on logic using TSVs

Cost of Future Scaling



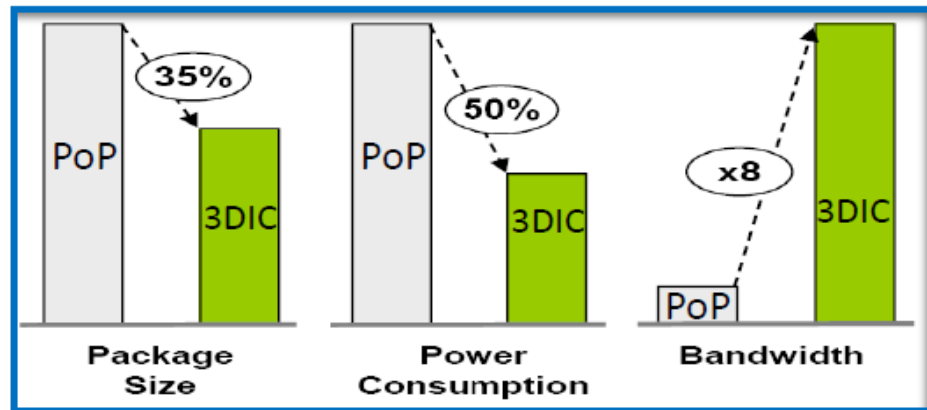
Reference: Global Foundries 2011

2011 rank	Company	Semi sales (\$B)
1	Intel	49.7
2	Samsung	32.7
3	TSMC	14.6
4	TI*	12.2
5	Toshiba	10.0
6	Qualcomm*	9.9
7	Hynix	9.4
8	Renesas	8.5
9	Micron	8.1
10	ST Micro	7.1
11	Broadcom*	7.1
12	AMD*	6.6

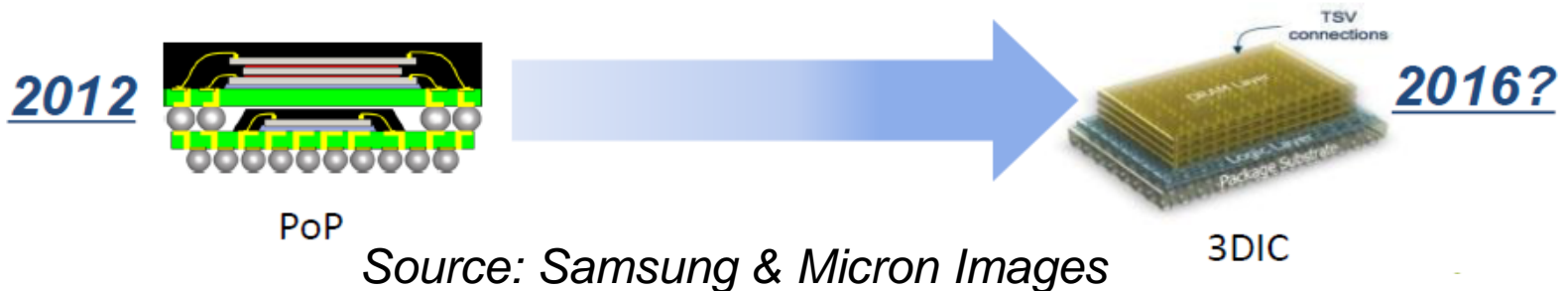
* Fabless or fab lite

Only a small number of companies can afford to build fine node fabs

The Governing Paradigm: More than Moore



Denser: "Higher Capacity/mm³"
Cheaper: "Lower Power Use"
Faster: "Quicker Data Access"



Source: Samsung & Micron Images

Temporary Bonding/Debonding

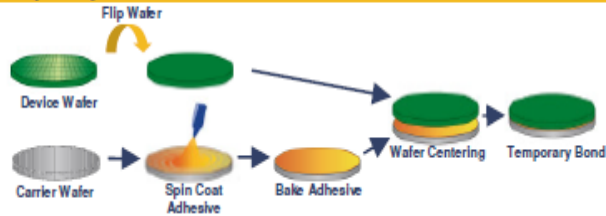
Temporary wafer bonding and debonding has emerged as challenging processes necessary for most 3D integration schemes. The selection of a suitable temporary bond process is the key to success. Through silicon via (TSV) processing places significantly higher technical demands on the bond process compared to MEMS or GaAs processing on smaller wafers.

The bond process must be able to withstand temperatures of up to 300C or more while at the same time be easily removed at room temperature, opposing objectives. It must be resistant to a wide range of semiconductor chemicals that it will contact, from solvents and acids to plating solutions and cleaning agents. Finally, it must have a very gentle debond process imparting the least amount of stress on a fragile thinner wafer with thicknesses goals of $\leq 25\mu\text{m}$.

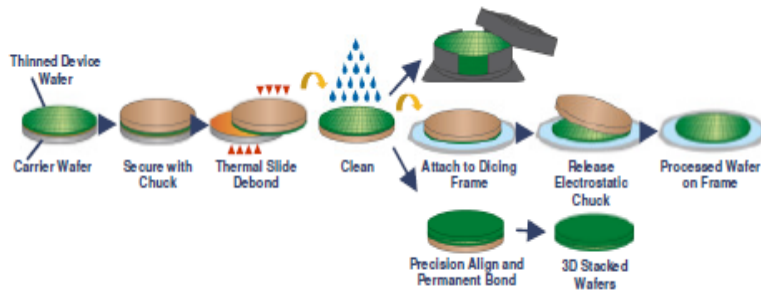
Brewer Science, Inc. WaferBOND HT10.10

Brewer Science Inc.: Materials/Process

Temporary Bond



Debond



Brewer's material uses an adhesive cast in solvent which is spin coated and baked much like photoresist.

Bonding is done in a vacuum chamber at moderate force (<8kN) and at ~200C.

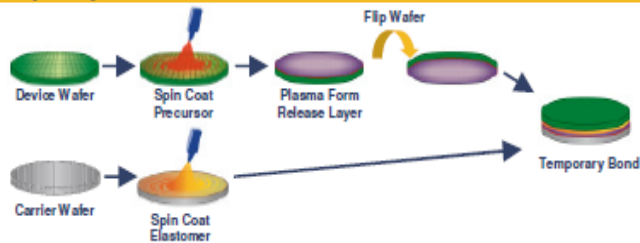
Debonding is conducted using a thermal-slide process where the wafer stack (carrier, adhesive and thinned wafer) is heated and the thinned wafer is slid off the carrier wafer.

The thinned wafer must then be cleaned using a solvent to remove the residue of the adhesive.

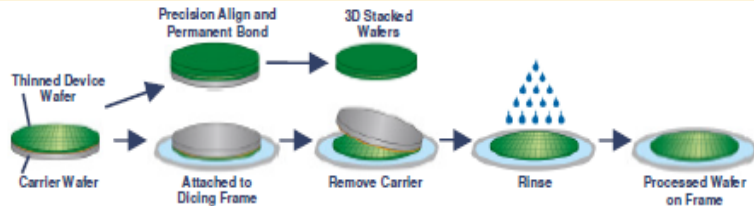
Thin Materials AG (T-MAT)

Thin Materials AG: Materials/Process

Temporary Bond



Debond

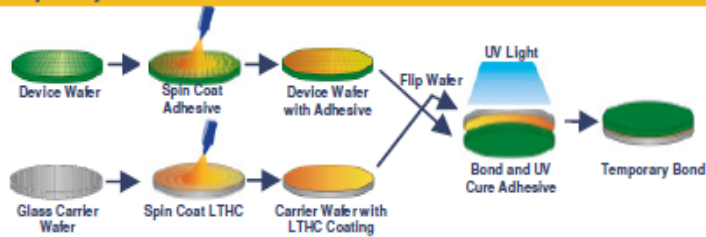


T-MAT's process uses a precursor spun on to the CMOS wafer. This is then converted via a simple PE-CVD process to form a release layer ~100 – 150nm thick. The elastomer used is a high temperature material cured at ~180C which joins the wafer to the carrier. Debonding can occur after the wafer stack is attached to a tape frame with the thinned wafer attached to the tape. One vacuum chuck is used to hold the thinned wafer via the taped side while another holds the carrier. Upon slight separation of the stack at one side, a debond wave moves across the stack separating the wafers and leaving behind the thinned wafer supported by the tape/frame.

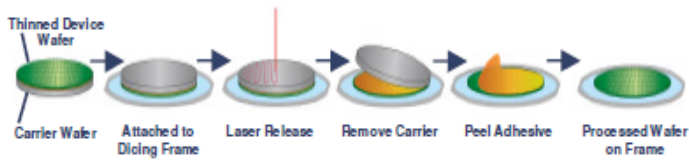
3M Wafer Support System

3M: Materials/Process

Temporary Bond



Debond



The use of laser release allows the selection of an adhesive based on the needs of the process. Higher thermal performance can be achieved while maintaining a low temperature, low stress method to remove the carrier. Key characteristics of the 3M process include room temperature bonding and debonding; high temperature capable adhesive; reliable support of the thinned wafer throughout the entire process; and no need for wafer cleaning after debond.

Conclusion

- First 3D stacked based products are beginning to emerge.
- Reference flows to build devices with TSVs and subsequent assembly are starting to converge.
- There are still technical challenges that need to be addressed:
 - Cost effective TSV formation
 - Thin wafer handling
 - Thermal management
 - Cost effective 3D stacking

Focus needs to be directed at a cost effective assembly solution, i.e. cannot make a low cost TSV that requires a very thin Si-substrate, but is impossible to handle and assemble.

Permanent Wafer Bonding

Wafer bonding got its start in the manufacture of MEMS, mostly for automotive applications. Microsystems such as accelerometers, micromirrors and gyroscopes require a sealed microcavity to protect the device from harsh environments, while allowing the mechanical function to be performed. Other devices such as infrared (IR) detectors or resonant devices required a vacuum-sealed package.

Permanent Wafer Bonding

Later, wafer bonding was used for MOEMS, systems combining optical and electrical functions, with applications as varied as hearing aids and IR focal plane arrays. Beyond MEMS and MOEMS, three other applications drive wafer bonding technology: wafer-level packaging, 3-D chip stacking and silicon-on-insulator (SOI) wafers. The myriad of applications has led to several bonding methods. Also, a new type of wafer bonding application is emerging that combines various materials as a means of designing novel devices. These custom-engineered substrates allow for combinations of materials that have been imagined for years, such as GaAs-on-silicon and InP-on-silicon for optoelectronic devices.

Permanent Wafer Bonding

Depending on the application, bonding requirements vary greatly. For MEMS, temperature and pressure uniformity across the wafer are essential, and wafers typically measure 75-150 mm. For SOI, neither high temperature nor force is applied. Instead, wafer cleanliness on the nanometer level is necessary, and 200 and 300 mm wafers must be accommodated. "The driving force for 300 mm was SOI on the one hand, and the other was 3-D interconnects.

Wafer-level Bonding

(Permanent step of 3D packaging)

For wafer-level 3D packaging, bonding accuracy and uniformity is important, as well as the co-planarity of the bonded wafers. Substrate bonding also allows more flexibility in the process than the alternative, die-level flip-chip bonding, because the environment can be controlled to use a process gas of the users choice with chamber pressures below atmosphere. Whereas flip-chip bonding is performed at room temperature and pressure. Wafer level bonding of semiconductor devices or sensors also protects the devices from possible contamination of subsequent processes such as dicing and die singulation.

Bonding Choices

Wafer bonding can be used to join any two flat mirror-polished clean surfaces with various crystallographic orientations and lattice constants. Typically temperature, force and/or an intermediate layer are used to facilitate bonding. Silicon direct, anodic, eutectic and Thermocompression bonding are common, with Cu-Cu bonding increasingly being used with ultrathin wafers for 3-D interconnects.

Anodic Bonding

Anodic bonding joins a silicon wafer with a glass wafer that contains a high concentration of alkali metal oxides (often Pyrex). At elevated temperature (200-500°C), a high-voltage electric field is applied, which dissociates the oxides and drives the metal ions into the glass. The process creates an oxygen-rich layer at the silicon-glass interface. The electric field forces the oxygen ions to the silicon surface, resulting in a strong, irreversible bond. In the case of silicon-to-glass, the anodic bond uses the conductive properties of the glass to create covalent bonds and a hermetic seal.

Eutectic Bonding

Eutectic bonds are used when a hermetic or vacuum seal is required, generally for sensors. It uses an intermediate bonding material that forms a eutectic alloy at a specific temperature, such as gold-silicon, gold-tin, or lead-silicon. The metal is usually deposited by plating, while the silicon source can be the wafer or CVD. Solid-liquid mixing occurs at temperatures slightly above the eutectic point and high contact force (40 kN). A hermetic solid seal forms upon cooling.

Eutectic Metal solutions for W2W Bonding

+ Al-Ge $T_e = 419C$
 $X_e = 28.4 \text{ at\%} - 51.8 \text{ wt\% Ge}$
 $\alpha + \beta$ simple eutectic microstructure

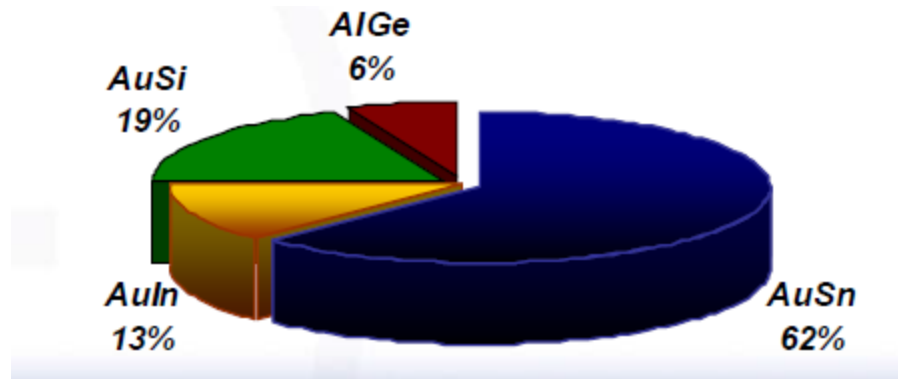
+ Au-Sn $T_e = 278C$
 $X_e = 29 \text{ at\%} - 20 \text{ wt\% Sn}$
 $\zeta' + \delta$ eutectic microstructure

+ Au-Si $T_e = 363C$
 $X_e = 18.6 \text{ at\%} - 3.16 \text{ wt\% Si}$
 $\alpha + \beta$ simple eutectic microstructure

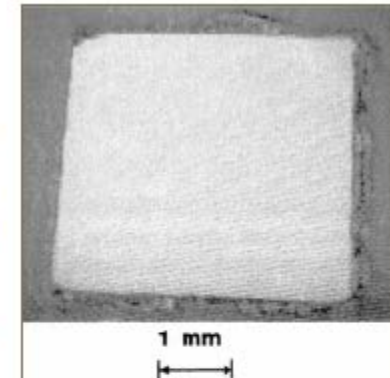
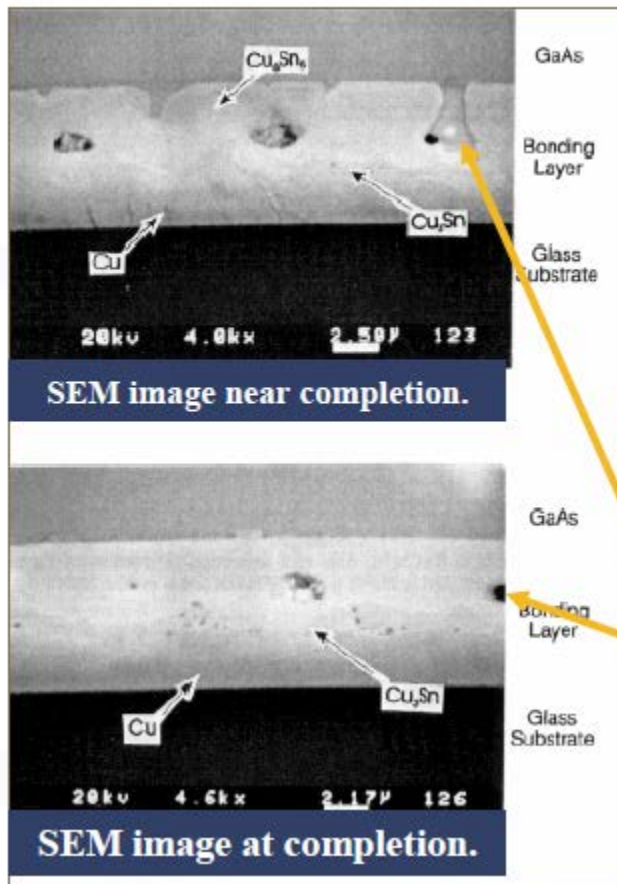
+ Cu-Sn $T_e = 231C$ + solid state diffusion
 $X_e = 25 \text{ at\%} - \sim 38 \text{ wt\% Sn}$
 $\eta + \varepsilon \rightarrow \varepsilon$ solid state reactions

+ Au-Ge $T_e = 361C$
 $X_e = 28 \text{ at\%} - 12.5 \text{ wt\% Ge}$
 $\alpha + \beta$ simple eutectic microstructure

+ Au-In $T_e = 156C$ + solid state diffusion
 $X_e = 55.3 \text{ at\%} - 41.9 \text{ wt\% In}$ final goal
 $\zeta + \delta$ simple eutectic microstructure



Cu-Sn Low T Solid State Bonds



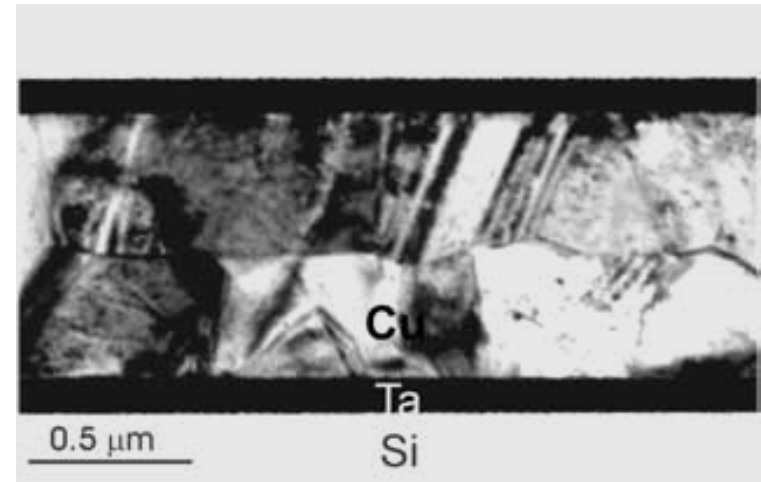
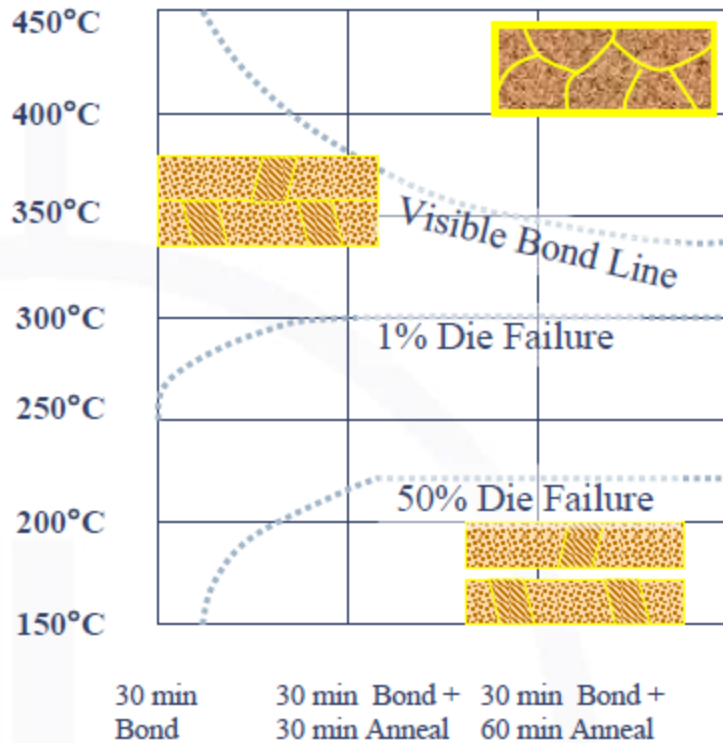
Acoustic image of interface after bonding.

- Cr-0.03um
- Sn-2.5um
- Cu-0.1um
- Au-0.1um
- Cu-4.4um
- Cr-0.03um

Thermocompression Bonding

Thermocompression bonding uses two similar materials (Cu-Cu) deposited onto a substrate either in a blanket form or patterned using photo masking processing. After a short process designed to remove native oxides, heat and pressure are applied to make a hermetic seal. Thermocompression bonding is used in hybrid circuit manufacturing, and is being used by some companies for 3-D interconnect fabrication.

Cu-Cu Bond Kinetics



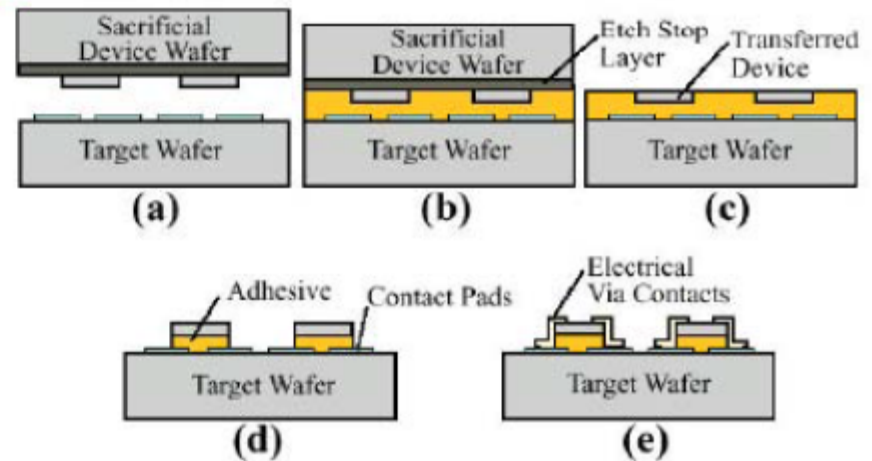
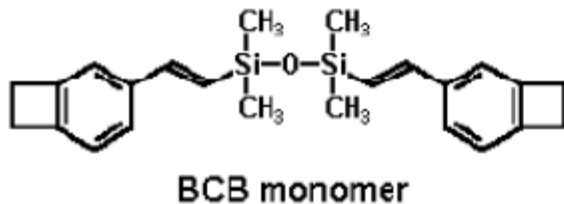
Adhesive Bonding

This bond requires a well controlled temperature and applied force with temperatures from 150° - 300° Celsius with forces from 0-8 Kilo- newton's to eliminate squeeze out of excess material. This is a good approach for mismatched substrates or permanent bonds at lower temperatures.

BCB Bond Example

Typical Applications for BCB Bonding

- + 3D Integration
- + CMOS Image Sensors
- + Layer Transfer Bonding



Schematics and images provided by Frank Niklaus, Royal Institute of Technology, Sweden.

SU-8 Bond Example

+ Applications

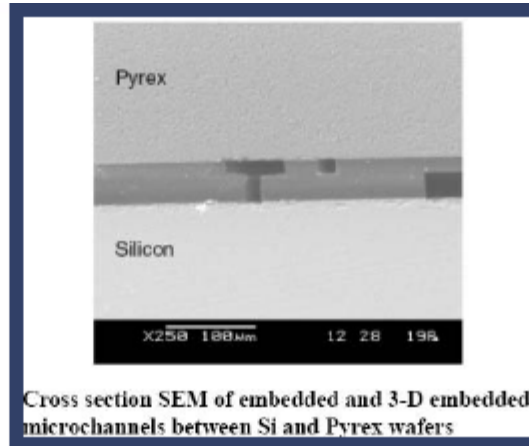
- Microfluidics
- μ TAS

+ SU 8 Benefits

- Excellent Adhesion to piezoelectric substrates (ZnO, AlN, etc)
- Vertical profiles
- Low moisture uptake
- Cost Effective

+ Several formulations available

- SU-8/3000 and SU-8/4000 enable bonding directly to silicon
- SU-8/3000 allows for patterned bonding between Si or glass



Cross section SEM of embedded and 3-D embedded microchannels between Si and Pyrex wafers



Silicon Direct Bonding

Silicon direct bonding, also called fusion bonding, uses applied temperature and pressure to join two materials, often an oxidized silicon wafer (the device wafer) and a silicon donor wafer. Later, the top wafer is cleaved or planarized to form an SOI wafer. In high-performance microprocessors, the silicon device layer is typically 500 nm or thinner, whereas SOI sensor wafers typically have $>2\ \mu\text{m}$ silicon layers. SOI wafers are sold by companies such as Wacker Siltronic (Burghausen, Germany), Soitec (Bernin, France), are the leading providers of SOI wafers to the semiconductor industry.

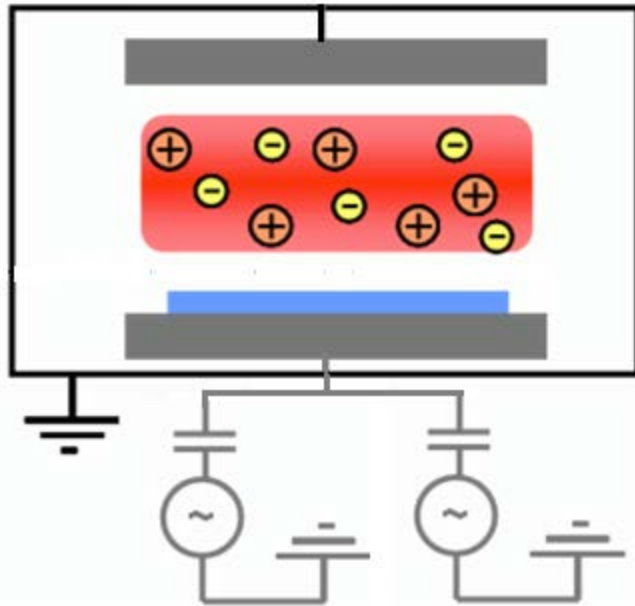
Silicon Direct Bonding

A key drawback to fusion bonding is the high-temperature anneal required to activate the bond. Alternatively, companies are using plasma processing to reduce annealing temperatures from $\sim 1000^{\circ}\text{C}$ to $200\text{-}300^{\circ}\text{C}$. The plasma alters the surface of the wafer, making it hydrophilic. Then it allows the wafers to become heterogeneous more readily with less temperature, so now we can perform fusion bonding on wafers at a reduced temperature.

Plasma Activation bond Theory

- Eliminate or reduce residual moisture at the interface.
- Provide chemical species needed for interface reaction and eliminate un-necessary intermediates.
- Catalyze reaction kinetics with near surface electric field via radicals with no residual plasma damage.
- Reduce or eliminate contamination and particles with a controlled environment.

TTS Source



High radical generation

Spacing of electrode > 4 cm

Biased controlled Ion rejection

Large process window due to decoupled source

Designed for optimum surface activation with very low chance of damaging wafer circuitry

Closing Statement

In the end, this change in direction that wafer to wafer or die to wafer bonding has enabled the semiconductor device manufacturers to continue the march for smaller more dense devices in a cost effective way. This will continue the movement forward at an incredible pace and complexity.