Transient Limiting Inductor Applications in Shunt Capacitor Banks

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1. INTRODUCTION

Fixed Inductors are often used in shunt capacitor installations in series with each phase of a capacitor bank. The inductors primary purpose is to limit transient currents during switching (inrush) or close in faults (outrush). In wye connected banks inductors have been placed between the bus and the capacitor switching device, between the capacitor switching device and the capacitor, or between the neutral end of each phase of the capacitor and the neutral point as shown in Figure 1.

![Figure 1. Illustration of example transient limiting inductor installations.](image)

Since the primary purpose of these fixed inductors is to limit transient currents associated with the capacitor bank, we name them: “Transient Limiting Inductors” (TLIs). These are fixed series inductors, not to be confused with “pre-insertion inductors” supplied with some capacitor switching devices, which are only temporarily in the circuit during a closing operation.

In the past 10–15 years capacitor bank faults have arisen where the capacitor was shorted out and the fault impedance was the TLI in series with the system back-up impedance. This situation gives rise to a Transient Recovery voltage (TRV) that is unmanageable by many circuit breakers, resulting in the circuit breaker failing to interrupt. Some kind of TRV mitigation is required to prevent this.

Some thought that by placing the TLIs in the neutral end of the capacitor bank, that the above failure scenario was eliminated. Placing the TLI in the neutral end does result in the TLI being bypassed in two fault scenarios (capacitor terminal to ground...
or phase to phase) but it doesn’t help for the possible fault which is shorting of the capacitor bank itself, phase to neutral.

This Committee Technical Report was written in response to a great amount of confusion in the Power industry surrounding the application of TLIs in shunt capacitor banks.

2. FIXED SERIES INDUCTORS (TRANSIENT LIMITING INDUCTORS)

2.1 Uses and Sizing

2.1.1 Limiting Inrush/Outrush Transients

Fixed Transient Limiting Inductors (TLIs) often called current limiting reactors (CLRs) have been used successfully to limit inrush currents during back-to-back capacitor bank switching. Typically, the value of these inductors is approximately several hundred microhenries. In addition, inductors for fault outrush current control may be applied, and are typically 0.5 - 2.0 mH. Previous research indicates, however, that these fixed inductors do not provide appreciable transient overvoltage reduction, unless they are very large. Very large inductors convert the capacitor bank to a true harmonic filter branch (often 13th harmonic or lower).

2.1.1.1 How to Size the Fixed Inductors

Sizing the fixed inductors should be done in such a way that at a minimum the inrush and outrush currents through the switching device will not exceed the device’s capability. Historically, the product of the current peak and frequency (I x f limits) defined in IEEE C37.06 standards [7] have been used to size transient limiting inductors for shunt capacitor banks. C37.06-2009 [6] no longer requires outrush inductors for circuit breakers having a Class C1 or C2 capacitance current rating as long as the peak current is below 2.6 x the short-circuit rating of the breaker.

There has been debate that the I x f limits published in IEEE standards are incorrect and have resulted in incorrect sizing of inductors when limiting the I x f to within the switching device’s “supposed” capability. SF6 and vacuum switching devices are not particularly frequency sensitive so their limits could be better expressed with peak current magnitude or peak current and duration.

Beyond concerns over the limitations of switching devices, TLIs can be sized to limit transient ground rise and control circuit coupling.
2.1.1.2 Switchgear Limits

Through 2014, IEEE standards provide a value of peak rated current and frequency of transients exposed to inrush currents from capacitor banks. For circuit breakers with a Class C1 or C2 rating IEEE Std. C37.06-2009 [6] provides a preferred rating, an Alternate 1 rating, an Alternate 2 and an Alternate 3 rating. The Alternate 2 and 3 ratings are an attempt to recognize the larger inrush capabilities of SF₆ circuit breakers. The Alternate 1 ratings are to limit inrush currents to 6 kA for vacuum circuit breakers to maintain their C2 capabilities. For Class C₀ circuit breakers, the transient inrush peak current on closing is to be less than 1.41 times the rated short-circuit current or 50 kA (whichever is less) and the product of the inrush current peak and frequency shall not exceed 2×10⁷ A-Hz. IEEE Std C37.06-2009 also provides commentary that for Class C1 or C2 circuit breakers exposed to outrush currents during fault conditions, the breaker should be expected to handle peak currents up to the close and latch rating of the circuit breaker twice during its life time without requiring maintenance of the contacts.

2.1.1.3 Capacitor Current Inrush limitations of Switchgear

Interest is rising in understanding the physics behind the inrush/outrush current limitations of switching devices. In a capacitive discharge, there is a fixed amount of energy available. The amount depends on the energy stored in capacitance just before a switching event, and the amount stored in the involved capacitors immediately after the event. For example, in a fault outrush event, all the energy stored in the capacitor banks is dissipated. In a back to back switching event, some of the initial stored energy is transferred to the previously un-energized capacitors, the remainder is dissipated.

The dissipated stored energy is split amongst:

- Resistive losses in the circuit external to the switching device
- Arc losses in the switching device:
  - Contact erosion
  - Heating of arc gasses
  - Shock waves

The shock wave energy does appear to be related to di/dt, however it cannot exceed the energy available. There is a threshold energy below which shock waves will not be damaging.

Arcs in oil are particularly effective at converting capacitive discharge into destructive shockwave shock wave energy. Arcs in Air and SF₆ create shock waves, but with much lower destructive energy than in oil, perhaps several orders of magnitude less.

Problems with the pre - 2014 di/dt method and limits are as follows:
• A minimum threshold energy is not considered.
• It derives from oil interrupter technology which is particularly shock wave sensitive.
• It does not account for non-oil technologies which have limitations other than shock waves.
• It has resulted in users installing series TLIs for SF₆ circuit breakers which may be unnecessary; and for oil circuit breakers perhaps larger than needed.
• Adding TLIs can result in TRV difficulties for SF₆ and air circuit breakers which would not exist without the TLIs.

The following is a practical example of the inappropriateness of the di/dt (Ixf) method/limits when capacitors are small:

Consider a 245 kV installation with two 5 nF CCVTs (or TRV shaping capacitors) on each side of a circuit breaker with 20 m (20 µH inductance) of buswork (and return path) between the CCVTs (or TRV shaping capacitors) as shown in Figure 2.

![Figure 2. Example case with closing a circuit breaker between two 5 nF CCVTs.](image)

The peak and frequency of the inrush current through the breaker could be calculated as follows:

\[
\text{Frequency} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{20\times10^{-6}\times (5\times10^{-9}/2)}} = 712 \text{ kHz}
\]

\[
\text{Peak} = \frac{245000\times\sqrt{2/3}}{\sqrt{L/C}} = \frac{245000\times\sqrt{2/3}}{\sqrt{20\times10^{-6}/(5\times10^{-9}/2)}} = 2.2 \text{ kA}
\] (1)

\[
I \times F = 712 \text{ kHz} \times 2.2 \text{ kA} = 1566 \text{ kAkHz (157x10⁷ A – Hz)}
\]
This I x f is over 78 times the formerly used limit of 2 x 10^7 A-Hz, and over 18 times
the 8.5 x 10^7 A-Hz used for “definite purpose” breakers. Similar installations do
exist in service and are known not to cause trouble for even oil circuit breakers.

The energy available is \( \frac{1}{2} \) the energy stored in one capacitor. If the breaker is closed
with one capacitor charged to the crest voltage and the other discharged, the
starting energy is \( \frac{1}{2} CV^2 \). At the end of the discharge, each capacitor will be charged
to \( \frac{1}{2} \) of the Peak voltage. The ending energy is \( \frac{1}{2} C \left(\frac{V}{2}\right)^2 + \frac{1}{2} C \left(\frac{V}{2}\right)^2 = C\left(\frac{V}{2}\right)^2 = \frac{1}{4} CV^2 \). Half of the initial energy is stored and the other half is dissipated. The
available energy is then \( \frac{1}{4} CV^2 \). Plugging in: \( 5 \text{nF}/4 \times (200 \text{kV})^2 = 50 \text{Joules} \). Only a
fraction of this energy can be converted into shock wave energy.

For the same case only with 13 nF CCVTs, the following would be the peak and
frequency:

\[
\begin{align*}
\text{Frequency} &= \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{20 \times 10^{-6} \times (13 \times 10^{-9}/2)}} = 441 \text{kHz} \\
\text{Peak} &= \frac{245000 \times \sqrt{2/3}}{\sqrt{L/C}} = \frac{245000 \times \sqrt{2/3}}{\sqrt{20 \times 10^{-6} / (13 \times 10^{-9}/2)}} = 3.61 \text{kA} \\
\text{I x F} &= 712 \text{kHz} \times 2.2 \text{kA} = 1567 \text{kA} \text{kHz} (157 \times 10^7 \text{A} - \text{Hz})
\end{align*}
\]

Since the peak voltage is the same, the energy available is directly proportional to
the ratio of the capacitances used in the 2 examples, i.e. 13 nF/5 nF = 2.6 so the
available energy is 2.6 \times 50 \text{ J} = 130 \text{ J}.

As shown in the two examples above, the I x f product for both the cases with the 5
nF CCVTs and the 13 nF CCVTs is identical (except for round-off error) even though
the ratio of capacitance and energy is more than double between the two cases. From lack of in-service trouble, we could conclude that 50 J and probably 130 J of
available energy may be below the threshold for damage.

Since in a capacitive discharge circuit, the di/dt reduces to \( \frac{U}{L} \), the value of the
capacitance doesn’t enter into the calculation of I x f.

A paper is being prepared: “The Impact of Capacitor Inrush/Outrush Currents on
Switchgear – Shock Wave and Contact Erosion”. The methodology is based on
fundamental arc physics and some simple laboratory tests. The purpose of the
paper is to demonstrate that typical capacitor inrush and outrush currents are not a
problem for SF6 circuit breakers. The concern on inrush is limited to contact wear.
TLIs may not be needed for such devices. Vacuum circuit breakers may still require
TLIs in capacitor applications mainly to insure they maintain their C1 or C2 restrike
performance.
2.1.1.4 Transient Ground Rise

Fast transients creating high \( \frac{di}{dt} \), due to capacitor fault outrush and back to back capacitor switching inrush currents, can result in transient ground rise if these currents are permitted to flow in the ground grid. For capacitor bank installations with high inrush and outrush currents, careful ground grid design and proper grounding practices can be used to mitigate excessive transient ground potential rise. Single point grounding is one method which can be used to eliminate most of the ground grid currents from back to back capacitor switching. Single point grounding is a technique where all neutrals of all capacitor banks at a given voltage in a substation are connected together and grounded at a single point. Single point grounding mitigates the impact of back to back switching transients as far as ground rise is concerned, but doesn’t eliminate transient ground rise for a fault outrush condition. However, back to back transients are frequent events and fault outrush is usually far less frequent. The operational aspects of transient ground rise can also be mitigated by connecting low voltage MOVs to local ground from low voltage circuits that are grounded outside the capacitor bank area. Other grounding practices such as peninsula grounding and direct neutral grounding [2] have also been successfully used in shunt capacitor bank installations.

TLIs can be used to reduce the \( \frac{di}{dt} \) and hence transient ground rise potentials between capacitor area grounds and remote grounds. If TLIs are installed to reduce transient ground rise, a detailed study is needed to determine how much the \( \frac{di}{dt} \) needs to be reduced for proper operation. Although this is a complex issue, it is often safe to assume that if the \( \frac{di}{dt} \) is reduced to the design short-circuit \( \frac{di}{dt} \) that would be low enough. Usually that requires a very large inductance TLI comparable to making the capacitor banks harmonic filters.

2.1.1.5 Control System Coupling

Induction into control systems can be minimized by proper shielding of control cables with the shields grounded at both ends and at critical points in the run. Also the routing of the control circuits must not compromise any special grounding design such as single point grounding or peninsula grounding. To minimize induction, the control circuits should not be run closely parallel to (i.e. underneath and in the same orientation as) phase conductors, or single point grounding conductors carrying capacitor related transient currents.

2.1.1.6 CT/LC Secondary Voltage

CT secondaries can be protected by appropriate MOVs preferably across each full secondary winding, and from the neutral point of the CT circuit to local ground. The MOVs need to be located as close as possible to the CT windings preferably in the CT secondary terminal box.
2.1.1.7 Other Limitations

All portions of the primary circuit through which inrush and outrush currents may flow must be capable of withstanding the peak currents expected. All ground connections should be as direct as possible and run so as to minimize extraneous ground wire inductance.

2.2 Drawbacks of Installing TLIs

2.2.1 Transient Recovery Voltages

When transient limiting inductors are installed for capacitor banks to limit inrush and outrush currents there is a potential that if a fault occurs in such a way that the inductor (transient limiting inductor) limits the fault current interrupted by the switching device (with minimal capacitance between the breaker and inductor) excessive TRV’s can be imposed on the circuit breaker. Refer to Figure 3 for an illustration of a reactor-limited fault for three example capacitor bank configurations. For each of the examples in Figure 3, a transient recovery voltage will be imposed on the circuit breaker that will often exceed standard circuit breaker TRV ratings [9] if no mitigation is installed to limit the transient recovery voltage component driven by the natural frequency of the inductor. This phenomenon is somewhat similar to a short line fault. Both cases are covered in [9].

Figure 3. Example capacitor bank configurations with a TLI-limited fault.
2.2.2 Tuning

Installing a TLI in a capacitor bank will create a series resonant circuit. One needs to be aware of existing harmonics (usually very high order) that might excite this resonant circuit and produce unwanted loading on the capacitor and TLI.

A simple single frequency filter consists of a shunt capacitor with a fixed inductance in series. This may be the intended design or may simply be a side effect of adding a transient limiting inductor to a capacitor bank installation. An example circuit is shown in Figure 4.

![Figure 4. Simple harmonic filter.](image)

Typically only odd harmonics propagate through the electric system. These are divided into positive (1,7,13), negative (5,11,17), and zero (3,9,15) sequence harmonics. The zero sequence or triplen harmonics will only circulate through a grounded system. Thus, single frequency filter banks for positive and negative sequence harmonics are typically operated wye-ungrounded, while filter banks for zero sequence harmonics should be operated wye-grounded.

This section provides a very basic look at simplified single-frequency filter banks, specifically for capacitor bank design and effects of tuning. IEEE 1531 [3] should be consulted for a more in depth treatment of harmonic filters.

2.2.2.1 Single Frequency Tuning

A single frequency filter is typically tuned to a particular harmonic current (n). At the tuning frequency the impedance of the bank is minimized allowing the specified harmonic current to flow. The following equation demonstrates how the inductance and capacitance are tuned to the harmonic number.

\[
\frac{n \omega L}{n \omega C} = 0
\]  

(3)
Where:

\[ \begin{align*}
  n & = \text{harmonic #} \\
  \omega & = \text{angular frequency} = 2\pi f \\
  L & = \text{total inductance in each leg (H)} \\
  C & = \text{total capacitance in each leg (F)}
\end{align*} \]

As shown in the equation above, the circuit inductance and capacitance is completely compensated. Only the resistance of the circuit is left to limit the flow of harmonic current.

A filter may also be tuned to a non-integer number. For example, a harmonic filter tuned to \# 5.2 is designed to eliminate most of the 5th harmonic current and will slightly reduce the 7th harmonic current as well. A shunt bank should never be tuned to the fundamental frequency, as the resulting fully compensated circuit would simulate a fault.

### 2.2.2.2 Avoiding Tuning Frequencies

Most capacitor banks are designed using standardized capacitor units. Thus, it is necessary to verify that the installation is not tuned unintentionally. If the fixed shunt bank capacitance is known, the fixed inductance value can be found for a specified harmonic \( n \).

\[
L = \frac{1}{n^2 \omega^2 C}
\]  

(4)

In order to avoid most tuned harmonic points. The capacitor bank can be tuned well beyond any harmonics that are present on the system. A conservative approach would be to ensure the reactor is tuned above the 13th harmonic. Solving the equation (4) for \( n \geq 15 \) would provide a maximum inductance value. Some inverters produce non-integer harmonics of a higher order around 23rd harmonic or higher. A detailed study may be required to see if it is necessary to avoid tuning to those frequencies.

### 2.2.2.3 Tuned Filter Bank Design

If the reactor is purposefully tuned to a specific frequency, then the whole filter installation must be further examined to ensure that there is adequate margin to accommodate additional harmonic currents. (See IEEE 1531 [3])

The capacitance can be found using the desired Mvar output of the bank \( Q \) at the system nominal voltage \( V_{SY} \).

\[
C = \frac{Q (n^2 - 1)}{V_{SY}^2 \omega n^2}
\]  

(5)
Where:

\[ Q = \text{rated filter power (Mvar)} \]
\[ V_{SY} = \text{phase-to-phase bus voltage (kV)} \]

System studies or measurements should be performed to find the maximum amount of harmonic current \( I_n \). The 60Hz thermal equivalent current circulating in each leg can be found by summing the harmonic and fundamental currents:

\[ I_{EQ} = \sqrt{I_1^2 + I_n^2} \]  
\[ (6) \]

Where:

\[ I_{EQ} = \text{Equivalent 60Hz rms Current (A)} \]
\[ I_1 = \text{Fundamental rms Bank Current (A)} \]
\[ I_n = \text{Maximum rms nth Harmonic Current (A)} \]

Multiple iterations may be required before the best capacitance and inductance values are found. An economic design would dictate that standardized capacitor cans are used while the fixed inductor would be custom built.

After determining the final capacitance and inductance values, the equipment ratings should be verified using the following equations:

\[ I_L = f_L \times I \]  
\[ (7) \]

Where:

\[ I_L = \text{Rated 60Hz Inductor Current (A)} \]
\[ f_L = \text{Current Margin, typ.} \geq 1.1 \]

\[ V_C = \frac{f_C \times I}{\omega C} \]  
\[ (8) \]

Where:

\[ V_C = \text{Rated Capacitor Bank Voltage (V)} \]
\[ f_C = \text{Voltage Margin, typ.} \geq 1.1 \]

2.2.3 Losses/Loss Evaluation and Initial Cost

Perhaps the most obvious drawback to use of TLIs is their initial cost.

Depending on the design details, there is the cost of the TLI itself, the possible cost of TRV mitigation and the cost of accommodating the TLI. It may be possible to mount the TLI on the Capacitor equipment rack. The mechanical loading needs to be considered in the rack design, particularly the wind loading. For Capacitor bank
installations higher than 245 kV, the TLI will need its own structure, foundation and insulators.

Secondly, the TLI will add power losses due to its insertion resistance. If the TLI has a large inductance, there will be a considerable voltage rise across it, possibly necessitating a higher voltage rated capacitor bank. The TLI will actually increase the VAR output of the capacitor bank due to the voltage rise across it overcoming the series VAR loss.

2.3 Where to Locate the Fixed Inductors

When installing transient limiting inductors (TLIs) for controlling inrush and outrush currents, the inductors need to be in series with each phase of the capacitor bank. The location of the inductor relative to the circuit breakers and capacitor bank (i.e., on the system or capacitor side of the switching device or on the system side or neutral side of the capacitor bank) does not matter in terms of limiting inrush and outrush currents as long as they are installed on each phase and in series with the capacitor bank. For example, if the three configurations shown in Figure 1.1 have the same size capacitor bank and TLIs then the inrush and outrush currents for each configuration will be similar. Note that technically it is also possible to distribute the transient limiting inductors throughout the capacitor bank (small inductors for each capacitor unit). This has usually proven to be a cost prohibitive solution. When tank type capacitors are used, individual inductors can more easily be accommodated in each tank and this is an effective solution.

Since about 2005 many have advocated installing the TLIs in the neutral end of the capacitor bank. A disadvantage is that the neutral end of the capacitor then must be insulated to support the full phase to ground voltage during an energizing condition and 2 x the phase to ground voltage for a restrike condition. For banks of higher voltage rating than 145 kV this can be prohibitive. It requires a taller capacitor block, and imposes higher foundation loads. Also, the additional neutral end insulation causes the fault probability to shift slightly away from a line end terminal to ground fault towards a line to neutral fault. This somewhat defeats the initial thinking of placing the TLIs at the neutral end. The above, concerns do not apply for ungrounded neutral capacitor banks. The consensus of the WG is that a neutral end location of the TLI can work, but it is not a preferred location. The use of a reduced end to end BIL with arrester protection for the TLI is applicable for any TLI location and not peculiar to the neutral end location.

2.4 TRV Delay Capacitors for the TLI

The installation of TLIs in capacitor bank applications limit the rate of rise of current, as explained in the paragraphs above, resulting in softening the impact of back to back switching by limiting current inrush and outrush. However, the arrangement changes the configuration of the circuit to the extent that it can affect
the circuit breaker performance due to the rate of rise of the transient recovery voltage during the circuit breaker attempt to clear the faults in the capacitor bank itself or between the capacitor bank and the inductor (see Figure 5 below).

![Diagram of a circuit with labeled components: Transient Limiting Inductor (TLI), C1 Capacitor Bank, Rs, Ls, Cstray, VS, and a symbol for an inductor with an inductive symbol above it.]

**Figure 5. Typical TLI installation in capacitor bank applications.**

When the circuit breaker interrupts the fault, the voltage potential across its contacts (TRV), equals the vector difference of the voltages on the line and load side of the opened circuit breaker contacts. As the voltage on the system (bus) side of the circuit breaker returns to the normal frequency and the systems' voltage rating, the voltage on the load side oscillates at a high frequency determined by the values of the TLI inductance (L) and the equivalent stray capacitance on the load side of the inductor (Cstray). The voltage on the load side can be estimated as follows:

\[ V_L = I_{sc} \times \omega L \]  \hspace{1cm} (9)

Where:

- \( V_L \) = peak TLI voltage in kilovolts
- \( I_{sc} \) = peak short-circuit current in kilo amperes
- \( L \) = inductance of the transient limiting inductor

The frequency of the oscillation is given by the equation:

\[ f = \frac{1}{2\pi \sqrt{LC_{stray}}} \]  \hspace{1cm} (10)

Where:

- \( f \) = frequency of oscillation (in Hertz)
- \( C_{stray} \) = stray capacitance on the inductor side of the circuit breaker

The capacitance, \( C_{stray} \), consists of the equivalent stray capacitance of; the inductor, the bus between the inductor and the circuit breaker including the phase to ground capacitance of the load side of the circuit breaker and the bus from the inductor to the point of fault. This capacitance typically sums to a small value of few hundreds of
picofarads, yielding to a frequency of oscillation of hundreds of kilohertz and, as a result, leading to a very high Rate of Rise of Recovery Voltage (RRRV) across the circuit breaker contacts. This phenomenon is known and such events have occurred in the past on different voltage levels throughout the utility industry and have been documented in numerous IEEE papers.

As equation 10 above suggests, the increase of $C_{stray}$ would decrease the frequency of the oscillation. The increase of $C_{stray}$ also decreases the RRRV of the TRV since the voltage across a capacitor is given by:

$$V = \frac{Q}{C}$$  \hspace{1cm} (11)

Where:

$Q$ = is the capacitor charge

From the formula above the voltage rate of change is:

$$\frac{dV}{dt} = \frac{1}{C} \frac{dQ}{dt} = \frac{I}{C}$$ \hspace{1cm} (12)

Where:

$I$ = is the current flowing through the capacitor. Higher capacitance results in slowing the voltage rise

Practical solutions to limit the TRV for these applications have been found by adding surge capacitors on the load side of the circuit breaker. The main locations for these capacitors are:

- Line to ground between the circuit breaker and TLI or
- Across the TLI

### 2.4.1 Location of TRV Delay Capacitors

#### 2.4.1.1 Line to Ground

A line to ground location can be used but it will require a fully insulated capacitor that will be under normal full voltage stress.

#### 2.4.1.2 Across TLI

This may be a more difficult mounting position but here the capacitor will only see significant voltage during transient events. One needs to calculate the tuning point of the TLI and its parallel capacitor to make sure that a higher order harmonic is not inadvertently magnified.
2.4.2 Sizing TRV Delay Capacitors

2.4.2.1 Voltage Rating

The voltage rating depends on the location. For line to ground connections the full system voltage rating will be required as well as full system BIL.

For a capacitor across the TLI, the voltage rating needs to be high enough to withstand the peak voltage during transient conditions including lightning transients, and breaker restrike events. The normal (steady state) voltage across the capacitor will be usually < 5% of the system voltage.

It is also possible to use an MOV across the TLI and capacitor to clamp the voltage and allow lower TLI and capacitor Insulation values. One must be careful that the MOV clamping voltage is not so low that it shorts out the TLI during inrush/outrush events.

2.4.2.2 Capacitance

The capacitance value will need to be determined by a TRV study for the circuit breaker. Capacitance is required to reduce the slope of the TRV from a fault where the TLI would be a major contributor to the fast portion of the TRV.

Normally one would look at the case where the capacitor bank is shorted and the fault impedance is the TLI and the system back up impedance. This applies regardless of where the TLI is located in the capacitor circuit. TLIs in the neutral end of a capacitor bank are not exempt from this.

3. REFERENCES


APPENDIX A

A.1 Overview of Capacitor Bank Switching Transients

Transient voltages and currents are a result of sudden changes within the electric power system. Opening or closing of a switch or circuit breaker causes a change in circuit configuration and the associated voltages and currents. A finite amount of time is required before a new stable operating point is reached. All transients are caused by either connection or disconnection of elements within the electric circuit or injection of energy due to a direct or indirect lightning strike or static discharge. [note: a restrike (or reignition) is reconnection of circuit elements with stored energy]

A.2 Isolated (Single) Capacitor Bank Switching Transients

Utility capacitor bank switching is a normal system operation and the resulting transient voltages and currents are usually not a problem for utility equipment. However, there is a possibility that these relatively low frequency transients can cause severe secondary transients if a customer has power factor correction capacitors or result in nuisance tripping of power electronic-based devices, such as adjustable-speed drives. Power quality problems related to utility capacitor bank switching include customer equipment damage or failure, nuisance tripping of adjustable-speed drives or other process equipment, transient voltage surge suppressor failure, and computer network problems.

Transient overvoltages and overcurrents related to capacitor bank switching are classified by peak magnitude, frequency, and duration. These parameters are useful indices for evaluating the effect of these transients on utility and customer equipment. The absolute peak voltage, which is dependent on the transient magnitude and the point on the fundamental frequency voltage waveform at which the event occurs, is important for dielectric breakdown evaluation. Some equipment and types of insulation, however, may also be sensitive to rates-of-change in voltage or current.

Energizing a shunt capacitor bank from a predominantly inductive source creates an oscillatory transient that can approach twice the normal system peak voltage (Vpk). The characteristic frequency ($f_s$) of this transient is given by the following expression:

$$f_s = \frac{1}{2\pi \sqrt{L_s C}} = f_{\text{system}} \times \sqrt{\frac{X_c}{X_s}} = f_{\text{system}} \times \sqrt{\frac{\text{MVA}_{sc}}{\text{Mvar}_{3p}}} = f_{\text{system}} \times \sqrt{\frac{1}{\Delta V}}$$  \hspace{1cm} (13)

Where:

- $f_s$ = characteristic frequency (Hz)
- $L_s$ = positive sequence source inductance (H)
$C$ = capacitance of bank (F)

$f_{\text{system}}$ = system frequency (50 or 60 Hz)

$X_s$ = positive sequence source impedance (ohm)

$X_c$ = capacitive reactance of bank (ohm)

$\text{MVA}_{\text{sc}}$ = three-phase short-circuit capacity (MVA)

$\text{Mvar}_{3\phi}$ = three-phase capacitor bank rating (Mvar)

$\Delta V$ = steady-state voltage rise (per-unit)

For example, the characteristic energizing frequency for a 4.8 Mvar, 13.8 kV distribution capacitor bank with source strength ($I_{3\phi}$) of 10 kA may be approximated using the following expression:

$$f_s = \frac{1}{2\pi \sqrt{L_s C}} = f_{\text{system}} \times \frac{X_c}{X_s} = f_{\text{system}} \times \sqrt{\frac{\text{MVA}_{\text{sc}}}{\text{Mvar}_{3\phi}}} = f_{\text{system}} \times \sqrt{\frac{1}{\Delta V}} \quad (14)$$

Where:

$$\text{MVA}_{\text{sc}} = \sqrt{3} \times 13.8 \text{kV} \times 10 \text{kA} = 239.02 \text{ MVA} \quad (15)$$

The steady-state fundamental frequency voltage rise for this case may be approximated using the following expression:

$$\Delta V = \left( \frac{\text{Mvar}_{3\phi}}{\text{MVA}_{\text{sc}}} \right) \times 100 = \left( \frac{4.8}{239.02} \right) \times 100 = 2.0\% \quad (16)$$

Relating the characteristic frequency of the capacitor bank energizing transient ($f_s$) to a steady-state voltage rise ($\Delta V$) design range provides a simple way of quickly determining the expected frequency range for utility capacitor bank switching. For example, a 60 Hz system with a design range of 1.0% to 2.5% would correspond to characteristic frequency range of 380 Hz to 600 Hz. For a shunt capacitor bank on a utility bus, feeder/cable capacitance and other nearby capacitor banks cause the energizing transient to have more than one natural frequency. However, for the first order approximation, this equation can still be used to estimate the dominant frequency.

Because capacitor voltage cannot change instantaneously, energization of a capacitor bank results in an immediate drop in system voltage toward zero, followed by an oscillating transient voltage superimposed on the fundamental frequency waveform. The peak voltage magnitude depends on the instantaneous system voltage at the instant of energization and can approach twice the normal system voltage. For a practical capacitor bank energization without trapped charge, system losses, loads, and other system capacitances cause the transient magnitude to be less than the theoretical 2.0 per-unit.
Typical magnitude levels range from 1.3 per-unit to 1.8 per-unit and typical transient frequencies generally fall in the range from 300 Hz to 1000 Hz. [note: distribution system capacitor energizations tend to produce lower overvoltages than bus connected transmission voltage capacitors] Figure 6 shows an example of a measured distribution system capacitor bank energizing transient voltage waveform that has a peak magnitude of 1.35 per unit and an energizing frequency of 540 Hz.

A.3 Back-to-Back Capacitor Bank Switching Transients

Energizing a shunt capacitor bank with an adjacent capacitor bank already in service is known as back-to-back switching. High magnitude and high frequency currents will flow between the capacitor banks when the second capacitor bank is energized. This current may need to be limited to acceptable levels for switching devices and current transformer burdens. Often, fixed series reactors (TLIs) are used with each capacitor bank to limit the current magnitude and frequency. Pre-insertion resistors and/or inductors may also be used with some types of switches. The frequency and magnitude of the inrush current during back-to-back switching depends upon the rating of the discharging capacitor bank, the impedance of the
discharging loop, and the instantaneous capacitor bank terminal voltage at the time of contact closure.

The impedance of the discharging loop is determined by the inductance between the capacitor banks, rather than the system inductance. This causes the magnitude of the inrush current to be much higher than for isolated capacitor bank energization. Typically, the inrush current lasts for only a fraction a power frequency cycle. Figure 7 shows an example measured distribution feeder capacitor bank back-to-back switching transient current waveform that has a peak magnitude of 602.4 amps and an energizing frequency of 2,040 Hz.

![Figure 7: Example of a measured feeder current during back-to-back switching.](image)

The high-frequency inrush current may exceed the assumed transient frequency momentary capability or peak withstand capability of the switching device (e.g., IEEE Std. C37.06 and IEEE Std. C37.012) as well as the $I^2t$ withstand of the capacitor fuses. It may also cause false operation of protective relays and excessive secondary voltages for current transformers in the neutral or phase of grounded-wye capacitor banks. The back-to-back inrush current must be evaluated with respect to the transient frequency momentary capability rating of the switch, as well as the $I^2t$ withstand of the capacitor fuses. If either of these ratings is exceeded, possible solutions to the excessive inrush currents usually involve:
• Adding current-limiting reactors (TLIs) to decrease the peak current and frequency of the oscillatory inrush current
• Adding pre-insertion resistors or inductors to the switching device
• Adding synchronous closing control to the switching device
• Switching the capacitor bank in smaller increments
• Selecting component ratings (e.g., circuit breakers, current transformer burdens, etc.) to withstand the inrush current characteristics

To control the substation ground mat transients due to the high-frequency inrush currents, where two or more grounded wye capacitor banks are at the same location, the capacitor bank neutrals may be directly connected, with a single connection to ground (single point grounding). Peninsular grounding has also been effective give reference IEEE C37.99, IEEE 1036.

A.4 Transient Outrush Currents during Nearby Faults

The concern for outrush currents exists when a fault occurs close to the capacitor bank substation and one of the substation circuit breakers must close into the fault (e.g., during a reclosing operation). The result is that a high-frequency, high-magnitude current may flow through a circuit breaker that may not be rated for that duty. The current magnitude and frequency must be evaluated with respect to the circuit breakers’ close and latch rating. Figure 8 shows a simplified system diagram that can be used for the evaluation of outrush reactor requirements. The primary consideration for capacitor banks is that there is sufficient impedance to adequately reduce the outrush current magnitude and (and sometimes frequency) to the desired levels.

It is important to note that some transient mitigation methods, such as pre-insertion devices or synchronous closing control, do not reduce outrush currents because they only operate when a capacitor bank switch is being closed. The full outrush current occurs when the resistors are bypassed.

Figure 9 shows an example of a simulated high frequency transient outrush current from a utility transmission capacitor bank into a nearby three-phase fault. The peak magnitude of the outrush current is approximately 16.7 kA and the frequency is 2.1 kHz.
Figure 8. System diagram for outrush current evaluation.

Figure 9. Example of a simulated capacitor outrush current during a power system fault.
Circuit breaker inrush current limitations are specified in ANSI Std. C37.06. (3 options available) These inrush limitations are sometimes applied to the outrush considerations. Since outrush to a close in fault is a rare occurrence, it is expected at most twice in the life of a breaker, it does not need to be treated quite the same way as inrush, which may be daily or more frequent. In 2009, C37.06 was revised to allow outrush current up to the peak current rating of a circuit breaker (2.6 \times \text{the short-circuit rating}) for circuit breakers with a Class C1 or C2 capacitance switching rating. Prior to this, lacking specific guidance, the industry had used the $I_{pk} \times f$ product (refer to the notes for Tables 1A, 2A, and 3A in ANSI Std. C37.06-2000). In many cases the $I_{pk} \times f$ product criterion is unnecessarily restrictive, particularly with non-oil circuit breakers and small capacitor bank ratings. Many installations have been made with smaller reactors than required to meet the $I_{pk} \times f$ limitation of ANSI Std. C37.06-2000. Simply limiting the outrush current into a fault to something less that the peak current capability of the switching devices where there are no oil circuit breakers involved and the substation grounding can withstand the higher transient currents, has often been done.

It is interesting to note that this $I_{pk} \times f$ product is independent of capacitor bank rating. In other words, the required series inductance is dependent only on the peak voltage when the circuit breaker closes into the fault. For three-phase capacitor banks, a reasonably conservative estimate of the peak outrush current is:

\begin{align*}
    f &= \frac{1}{2\pi \sqrt{L_{eq} C_1}} \quad \text{(17)} \\
    I_{pk} &= V_0 \sqrt{\frac{C_1}{L_{eq}}} \quad \text{(18)} \\
    I_{pk} \times f &= \frac{V_0}{2\pi L_{eq}} \quad \text{(19)}
\end{align*}

Where:

- $I_{pk}$ = peak current, kiloamperes
- $f$ = frequency of outrush transient current
- $V_0$ = initial voltage on $C_1$
- $L_1$ = self-inductance of $C_1$
- $L_2$ = inductance between capacitor bank and fault
- $L_{eq} = L_1 + L_2$
- $\text{KVA}_C$ = Capacitor bank rating, three-phase kVar
- $C_1$ = total bank capacitance (microfarrads)
- $L$ = Inductance per phase between capacitor bank and fault (microhenries)
With parallel capacitor banks, there are a number of different ways to configure the capacitor banks and required series inductors (TLIs) if required. A few of the options are shown in Figure 10. Each option has advantages and disadvantages.

**Figure 10. Inrush and outrush reactor alternatives.**

1) **Option 1: Separate TLIs for inrush and outrush requirements.** When a larger TLI is needed for outrush, a common TLI for limiting outrush current, in addition to smaller TLIs for inrush current limiting, may be the optimum configuration.

2) **Option 2: Series TLIs rated for inrush and outrush in series with each capacitor bank.** If the TLI cost is not significantly dependent on its millihenry rating, then this option may be more economical than Option 1. However, with two equal capacitor banks in parallel, the TLI millihenry value required to control outrush may be more than double the single capacitor bank rating.

3) **Option 3: TLI for outrush only, switching device limit inrush.** If inrush current for back-to-back switching can be limited to acceptable levels without TLIs, this is probably the most economical configuration. Closing resistors, pre-insertion inductors or a closing control to close the contacts near voltage zeros are common alternate methods to limit the inrush current. The single TLI is used to is used to limit outrush currents to
acceptable levels. A disadvantage of this option is the high-current magnitude and frequency that can occur in the event of a restrike on opening.

For circuit breakers with C1 or C2 capacitor switching ratings, the new limitation in IEEE C37.09-2009 of keeping the peak outrush current below $2.6 \times$ the short-circuit current rating of the breaker, effectively eliminates the need for outrush inductors for many installations based on circuit breaker limitations alone.

Traditionally, when evaluating outrush, closing outrush was investigated. A line breaker was closed into a fault with a capacitor bank on the source side. This can result in contact burning and for vacuum breakers, contact welding. A somewhat different form of outrush can occur on opening,[20] We call it “reignition outrush”. From the perspective of transmission line circuit breakers during fault interruption, the presence of one or more capacitor banks represent a large source side capacitance and also a source of outrush currents. Both source side capacitance and outrush currents influence the fault interrupting process and may also influence the fault interruption time. Such a case is illustrated in Figure 11.

![Figure 11. Transmission line circuit breaker interrupting a fault near a capacitor bank.](image-url)
Transmission line circuit breaker (CB) interrupts a fault(s) on the transmission line. Assuming that the harmonic distortion is below 5%, the capacitor bank \((C_1)\) modifies the source side TRV to a 1-cos waveshape with a higher peak than the values given in IEC 62271-100 [2] or IEEE C37.06 [3]. For this phenomenon to occur the capacitor bank must be at the same voltage level and not connected to the bus by cable or overhead line.

When a fault occurs on the line, the capacitor bank will discharge into the fault through the closed circuit breaker (outrush). During interruption, the low \(\text{du/dt}\) of the modified TRV waveshape may result in a shorter minimum arcing time than demonstrated during the type tests. Arcing times shorter than the minimum arcing time may result in reignition of the circuit breaker and the capacitor bank will discharge into the fault again (reignition outrush). The contribution of the capacitor bank depends on the instantaneous voltage at the time of re-ignition and the inductance \((L_1 + L')\) between the capacitor bank and the fault. In the extreme case, the voltage just prior to breakdown can exceed 2 p.u. That would make the outrush current 2 times a closing outrush. The large outrush current can have a substantial frequency (several kHz) and it will create additional current zeros. Depending on the type of circuit breaker used (e.g. vacuum, oil, air or SF6) it may interrupt at one of the high frequency current zeros. Such an interruption is associated with overvoltages. Adding inductance into the circuit will limit the outrush current and frequency, but may result in an easier switching case for the circuit breaker (i.e. it may now be able to interrupt in one of the high frequency current zeros) creating overvoltages. The overvoltages could lead to additional high energy reignitions and ultimately a failure to interrupt. Any surge arresters on the bus or capacitor side could experience capacitor bank discharge from reignition outrush and interruption, from the prospective overvoltage.

Although the events described above are theoretically possible, and have been demonstrated in power lab tests [20], there is no documented evidence of such an overvoltage event occurring in actual power system service.

The impact of reignition outrush on a circuit breaker is quite different than a closing outrush, or normal switching inrush. The contacts are opening, not closing so contact welding would not be expected to occur, nor would contact wear from closing contact “chattering”. The \(\text{di/dt}\) on a reignition outrush could be 2 \(\times\) that of a closing outrush which could result in a more severe shock wave for an oil circuit breaker during a reignition outrush event.

The \(\text{di/dt}\) capability of bulk oil breakers is believed to be more than two times the 20 kA kHz limit for general purpose oil breakers recommended by standards. This is based on the difference between a general purpose oil breaker and a “definite purpose” oil breaker being the presence of high ohmic value opening resistors. On closing, these resistors only reduce the impact of inrush to about 80%, because they have a high ohmic value. So from a closing point of view, there is little difference between a definite purpose oil breaker and a general purpose oil breaker.
Historically, the general purpose oil breaker without the opening resistors, was never tested for capacitive inrush duty.

The likelihood of a reignition outrush occurring depends on the fault parameters, the circuit breaker performance, and the precise timing of the contact opening against the current zeros. It is estimated that the likelihood of a reignition outrush of > 1.0 p.u. occurring is <10% for a close in fault. This is based on an assumption that only a narrow timing window of about 1 ms will result in a reignition voltage above 1.0 p.u. A close in fault is also a rare occurrence, as are short-circuit currents close to the breaker rating.

Based on good field performance, and the small likelihood of a severe reignition outrush occurring, it is recommended that closing outrush continue to be the design base for outrush analysis. When the peak current rating of the breaker (2.6 x Short-Circuit Rating) is used as the outrush limit, a risk assessment should be made concerning the likelihood of reignition outrush during clearing of a close in fault. A reignition outrush could be up to 2 x a closing outrush. If reignition outrush is taken into account, the design base for the closing outrush analysis should only be ½ of the breaker’s peak current capability for the outrush limit. (i.e. 1.3 x Short-Circuit Rating).

A.5 Transient Overvoltages from Capacitor Bank De-Energizing and Restrikes

When a capacitor bank is de-energized the capacitor will retain a DC trapped charge equal to the voltage at the time of current interruption. Because the current is close to 90 degrees out-of-phase to the voltage, at the time of current interruption the voltage will be at a peak and therefore a trapped charge of near 1.0 per-unit will remain on the capacitor bank. After current interruption, the system voltage continues (at 60 Hz or 50 Hz power frequency) on the source side of the switching device while the DC trapped charge remains on the capacitor bank side of the device. Because the time constant of the capacitor bank discharge is on the order of 40 s, the DC trapped charge drains very slowly. For a grounded wye capacitor bank, one half cycle after current interruption (8.33 ms for 60Hz or 10 ms for 50 Hz) the voltage across the switching device will be near 2.0 p.u. For an ungrounded capacitor bank, switched with a device where the time difference between poles is <90 electrical degrees, the recovery voltage will be 2.5 p.u. If a switching device with >210 electrical degrees between poles is used, the recovery voltage can reach 4.1 p.u. If the dielectric withstand of the contact gap of the switching device has not had adequate time to recover (or if local stress enhancements have compromised the dielectric strength) when the 2.0 p.u. (2.5 p.u. or 4.1 p.u.) is imposed across the contacts, a dielectric breakdown can occur and current will start to flow again. This is known as a restrike if the voltage breakdown occurs longer than the first ¼ cycle following current interruption. A breakdown with < 1.0 p.u. voltage is called a reignition if breakdown occurs during the first ¼ cycle following current interruption.
Refer to Figure 12 for an illustration of a single restrike on a grounded capacitor bank.

Figure 12. Illustration of a single restrike.

If a restrike occurs near one half cycle following interruption, peak transient overvoltages more severe than those from normal capacitor bank energizing can occur because the voltage collapsed across the switching device is near 2.0 p.u. where for normal capacitor bank energizing it is 1.0 p.u. Theoretically, restrikes can lead to overvoltages across the capacitor of 3.0 p.u. total for a single restrike. For some switching devices, if a restrike occurs and the resulting inrush current following the restrike is interrupted multiple restrikes can occur leading to voltage escalation and much higher overvoltages. Refer to Figure 13 for an illustration of a multiple restrike on a grounded capacitor bank. Figure 14 provides another illustration of a restrike where multiple restrikes occur on successive voltage peaks (½ cycle intervals) with no voltage escalation.
The probability of having a restrike on a switching device is dependent on the device type and design. Many devices in use today for capacitor switching are classified as having a low or very low probability for a restrike (Class C1 or C2). Mitigation techniques such as controlled opening [synchronous-open control] can
be used to further reduce the probability of restrikes, and surge arresters are often applied to protect system equipment in the event that a restrike occurs.
APPENDIX B

B.1 Capacitor Bank Switching Transient Mitigation Methods

The devices currently available for transient overvoltage control either attempt to minimize the transient overvoltage (or overcurrent) at the point of application, or limit (clip) the overvoltage at local and remote locations. These devices include:

- Pre-insertion devices (resistors and/or inductors)
- Synchronous closing control (also known as zero voltage closing)
- Fixed inductors/reactors
- Surge arresters (metal oxide varistors – MOVs)

Previous studies (digital simulation and Transient Network Analyzer [TNA]) have suggested that the effectiveness of these control methods is system dependent, and that detailed analysis is required to select the optimum transient mitigation scheme. While often justifiable for large transmission applications, analysis of distribution system capacitor applications is rarely performed, and in general, capacitor banks are installed without transient overvoltage control.

Each of these transient control methods has various advantages and disadvantages in terms of transient overvoltage reduction, cost, installation requirements, operating/maintenance requirements, and reliability. Some of these techniques may be useful in controlling the transients when re-energizing a capacitor bank before the voltage has decayed to near zero.

B.2 Pre-Insertion Devices

A pre-insertion impedance (e.g., resistor or inductor) provides a means for reducing the transient currents and voltages associated with the energization of a shunt capacitor bank. The impedance is shorted-out (bypassed – refer to Figure 15) shortly after the initial transient dissipates, thereby producing a second transient event. The insertion transient typically lasts for a small fraction of one cycle of the system frequency. The performance of a pre-insertion impedance is evaluated using both the insertion and bypass transient magnitudes, as well as the capability to dissipate the energy associated with the event, and repeat the event on a regular basis. Pre-insertion resistors and high-loss pre-insertion inductors are one of the most effective means for controlling capacitor bank energizing transients.
The optimum resistor value \( R_{\text{optimum}} \) for controlling capacitor bank energizing transients depends primarily on the capacitor bank rating and the source strength. It should be about equal to the surge impedance \( Z_s \) formed by the capacitor bank and source impedance and it may be approximated using the following expression:

\[
R_{\text{optimum}} = \sqrt{\frac{L_s}{C}} \quad (20)
\]

Where:

- \( L_s \) = positive sequence source inductance (H)
- \( C \) = capacitance of bank (F)

This value results in a slightly underdamped insertion transient. For example, the optimum resistor rating \( R_{\text{optimum}} \) for a 4.8 MVar, 13.8 kV distribution capacitor bank with a source strength \( I_{3φ} \) of 10 kA may be approximated using the following expression:

\[
R_{\text{optimum}} = \sqrt{\frac{2.11 \text{ mH}}{66.86 \mu\text{F}}} = 5.62 \text{ ohms} \quad (21)
\]

The positive sequence source inductance \( L_s \) and the capacitance of the bank \( C \) may be determined using the following expressions:

\[
L_s = \frac{kV/\sqrt{3}}{2\pi f_{\text{system}}} = \frac{13.8/\sqrt{3}}{10} = 2.11 \text{ mH} \quad (22)
\]
\[
C = \frac{\text{Mvar}}{2\pi f_{\text{system}} \times \text{kV}^2} = \frac{4.8}{2\pi \times 60 \times 13.8^2} = 66.86 \mu\text{F}
\] (23)

Where:

- \(L_s\) = positive sequence source inductance (H)
- \(C\) = capacitance of bank (F)
- \(\text{kV}\) = phase-to-phase rms bus voltage (kV)
- \(f_{\text{system}}\) = system frequency (50 or 60 Hz)
- \(\text{MVA}_{\text{sc}}\) = three-phase short-circuit capacity (MVA)
- \(I_{\text{sc}}\) = three-phase short-circuit current (kA)
- \(\text{Mvar}\) = three-phase capacitor bank rating (MVAr)

Pre-insertion inductors, which were traditionally used primarily for overcurrent control for back-to-back capacitor switching applications also provide transient overvoltage magnitude reduction. The degree of overvoltage reduction achieved is largely determined by the relative size of the source inductance and the resistance and inductance of the pre-insertion inductor. Pre-insertion inductors are generally very effective for overvoltage reduction if the inductance is equal to or greater than the source inductance. Pre-insertion inductors with high resistance further increase reduction in overvoltages by increased damping of the oscillatory transient portion of the capacitor-switching voltage transient.

Power ratings for pre-insertion devices need to include the transient inrush and power frequency currents for the duration of the pre-insertion period. They should also have some margin for power frequency and harmonics beyond the pre-insertion time.

Figure 16 shows an example of a transient simulation for energization of a substation capacitor bank without and with a pre-insertion resistor. For the studied system, the maximum energizing transient overvoltage is reduced from 1.77 per-unit to 1.29 per-unit with addition of a 6.4 ohm pre-insertion resistor.
B.3 Controlled Closing (Point on Wave Closing Control)

Controlled closing is independent contact closing of each phase near a voltage zero, as illustrated in Figure 17. To accomplish closing at or near a voltage zero (avoiding high prestrike voltages); it is necessary to apply a switching device that maintains a dielectric strength sufficient to withstand system voltages until its contacts touch. Although this level of precision is difficult to achieve, closing consistency of ±0.5 milliseconds is possible. Previous research has indicated that a closing consistency of ±1.0 millisecond provides overvoltage control comparable to properly rated pre-insertion resistors.

The success of a synchronous closing scheme is often determined by the ability to repeat the process under various (e.g., system and climate) conditions. Adaptive, microprocessor-based control schemes that have the ability to learn from previous events address this concern. The primary benefits of this capability are the control’s ability to compensate for temperature induced differences in making time, (and in some cases, idle time). This can result in increased reliability (less maintenance).

Fully discharged grounded capacitor banks are controlled by closing the three phases at three successive phase-to-ground voltage zeros (60° separation). Fully discharged ungrounded banks are controlled by closing the first two phases at a phase-to-phase voltage zero and then delaying the third phase 90 degrees (phase-to-ground voltage zero).

Figure 18 shows an example of a transient simulation for energization of a substation capacitor bank without and with synchronous closing control. For the studied system, the maximum energizing transient overvoltage is reduced from 1.54 per unit to 1.11 per unit with a +1.0 millisecond closing error.

Figure 16. Illustration of the effect of a pre-insertion resistor during capacitor bank switching.
B.4 Surge Arresters

B.4.1 Uses

Surge arresters (e.g., metal oxide varistors [MOV's]) can limit transient voltages to the arrester's protective level (maximum switching surge protective level, typically 1.8 - 2.5 per-unit) at the point of application. The primary concern associated with
surge arrester application is the energy duty during a capacitor bank switch restrike. Although a rare occurrence, a switch restrike generally results in the highest arrester duty for arresters located near the switched capacitor bank. In addition, remote arresters (including low voltage customer applications) may be subjected to severe energy duties if voltage magnification occurs.

The energy duty requirements for arresters near capacitor bank locations depend on the ratings of the capacitor bank(s) and arresters. In general, the most severe duty during a switching event for an arrester near a capacitor bank occurs during a capacitor bank switch restrike. This is due to the trapped charge on the capacitor bank at the instant the restrike occurs, resulting in a greater magnitude of the transient voltage oscillation. Figure 19 illustrates the voltage and current waveforms for a single capacitor bank switch restrike.

![Figure 19. Illustration of a single capacitor bank switch restrike.](image)

Arresters across a TLI can allow a reduced insulation level to be used for the TLI. When transient limiting inductors are installed in the neutral of capacitor banks surge arresters can be applied across the inductor for protection of the inductor and capacitor bank neutral under switching and lightning events. When this is done studies should be performed to determine proper coordination between the arresters protective level and the anticipated overvoltages across the arrester. It should be verified that under switching events such as capacitor bank energizing (inrush currents) and re-closing into a close-in fault (outrush currents) the surge arresters do not short-out the inductor resulting in excessive inrush/outrush currents.
B.4.2 Drawbacks

The primary drawback of adding surge arresters is the addition of a potential point of failure. When a surge arrester fails, the usual failure mode is a short-circuit which could result in a line-to-ground fault in the substation which could in turn lead to other potential problems for adjacent equipment such as failure to interrupt the fault current.

B.4.3 Where in the Circuit to Locate the Surge Arresters

Surge arresters can be located in the following positions as shown in Figure 20:

- Bus side of the capacitor switching device
- Bus side of the TLI
- Capacitor side of the TLI
- Across the TLI

![Diagram](image)

**Figure B.6 – Example locations for surge arrester placement.**

Each of the locations above have been successfully used when proper insulation coordination studies have been performed for the substation, but each potential location has its own advantages and disadvantages. The table below shows a comparison of some potential advantages and disadvantages for each location.
<table>
<thead>
<tr>
<th>Location of Arrester</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
</table>
| Bus Side of Switching Device | - Provides protection for switching device from lightning/switching surges when open  
- Provides protection for TLI from fast front surges (e.g., lightning) | - Provides less protection for the capacitor bank because of voltage rise across TLI                      |
| Bus Side of TLI     | - Provides protection for TLI from fast front surges                         | - Provides less protection for the capacitor bank because of voltage rise across TLI                      |
| Capacitor Side of TLI | - Provides best protection for the capacitors                                 | - Provides less protection for the TLI from fast fronted surges (e.g., lightning)  
- If surge arrester fails to ground, high rate-of-rise TRV's can be imposed on the breakers |
| Across TLI          | - Provides protection for the TLI from lightning/switching surges             | - Does not protect the capacitor bank from lightning/switching surges  
- Can reduce TRVs from reactor-limited faults  
- Arrester does not see full line-to-ground voltage during normal operation |

**B.4.4 How to Size the Surge Arresters**

The size and location of the surge arresters should be determined in an insulation coordination study for the substation considering the desired insulation levels, location, and rating of surge arresters. Furthermore, the potential energy dissipated by the arrester should be calculated in the event of a restrike during capacitor bank de-energization. IEEE Std C62.22-2009 “IEEE Guide for the Application of Metal-Oxide Surge Arresters for Alternating-Current Systems” provides guidance for selecting surge arresters to protect the substation equipment including shunt capacitor banks.
APPENDIX C

Example 230kV Capacitor Bank TLI Study

C.1 Terminology

The inductor placed in series with an isolated (single) capacitor bank is usually installed to control the magnitude of outrush current from the capacitor bank to a breaker closing into a fault. Often, as in the case of this 230kV example, this is a line breaker closing into a close in fault on its terminals.

These inductors are referred to as:

- “Damping Reactors” this is IEC terminology
- “Current Limiting Reactors (CLRs)” common usage in the USA, but also applies to larger inductors used to limit fault current magnitudes.
- “Transient Limiting Inductors” (TLI) this is the Capacitor Subcommittee’s choice since the terminology “reactor” is somewhat archaic.

C.2 Introduction

What problem is trying to be solved in using a TLI?

Capacitor bank discharge current “Outrush” through a closed breaker is not harmful to the breaker unless the current exceeds the peak current capability of the breaker (2.6 x short-circuit rating).

Technically, the Capacitor discharge current will add to the 60 Hz short-circuit current. However, because the outrush current frequency is typically 30x or more than 60 Hz, and the capacitive outrush damps out in a few milliseconds, the 60Hz fault current component will only add a few percent to the peak current, and for purposes of simplicity will be ignored.

IEEE Standard C37.06-2009 clause 7.4 note (8) [found on page 32] states:

“(8) For Class C1 and C2 circuit breakers exposed to transient inrush currents from nearby capacitor banks during fault conditions, the capacitance transient inrush peak current shall not exceed the close and latch (peak withstand) capability of the circuit breaker. This is considered an infrequent event, and therefore the circuit breaker should be expected to handle this duty twice in its life time without requiring maintenance of the contacts.”

Thus for SF₆ breakers the breaker limitation on outrush through a closing breaker is the same as for a closed breaker: The peak current magnitude must not exceed 2.6 x the short-circuit rating of the breaker. There is no limitation on frequency of the outrush current.
C.3 Equations for Calculating the Outrush Current

When the Example 230 kV Capacitor is installed, all of the 230 kV Circuit breakers will be SF₆ puffer type with no arc assist, and with a 63 kA short-circuit rating. All are class C1 capable. Note (8) under clause 7.4 of IEEE C37.06-2009 [found on page 32] applies. Therefore, the peak outrush current must be limited to 2.6 x 63 = 163.8kA. While it is true that the Capacitive discharge will be added to the 60Hz fault current, the outrush current usually has a frequency in the range of 30 (or more) x 60 Hz and damps quickly. Thus the outrush current is mostly over before the 60 Hz fault current amounts to much. For simplicity, we will ignore the 60 Hz component.

The outrush current can be modeled as a series RLC circuit. The example capacitor is a grounded wye so we can look at one phase.

The C is provided by the capacitor bank.

\[
C = \frac{\text{Var}}{\omega V^2}\]  \hspace{1cm} (24)

Where:

- \(C\) = capacitance in microfarads
- \(V\) = rms kV
- \(\omega = 377\) (for 60Hz)

Note: If Var is three-phase, \(V\) is line to line kV
If Var is single phase, \(V\) is line to ground kV

To calculate the outrush current, one needs the capacitance of the bank as well as the total inductance (\(L\)) of the series circuit. The inductance (\(L\)) is the sum of bus work inductance, connections inductance (including the neutral connections, the capacitor bank self inductance, and any added discrete inductance (the TLI when applicable).

- For typical 230 kV bus and connections, assume 0.3 \(\mu\)H/foot.
- For a 230 kV cap bank assume 10 \(\mu\)H for the bank itself.
- [If you want to get fancy you can calculate the bank inductance. A capacitor unit is 1.0 \(\mu\)H, String/wiring is 0.4\(\mu\)H/ft.]

Since the circuit is under-damped, for conservatism, we will ignore the resistance when calculating the peak current and frequency. (The resistance will lower the peak and depress the frequency slightly)

\[
I_{\text{peak}} = V_{\text{peak}} x \sqrt{\frac{C}{L}}\]  \hspace{1cm} (25)
Where:

\[ C = \text{capacitance in Farads} \]
\[ L = \text{the inductance in Henries} \]
\[ V_{\text{peak}} = \text{the crest of the voltage which can be calculated as follows:} \]

\[ V_{\text{peak}} = V_{L\text{-RMS}} \sqrt{\frac{2}{3}} \]  

(26)

The frequency of the outrush current can be calculated as follows:

\[ f = \frac{1}{2\pi \sqrt{LC}} \]  

(27)

**C.4 Outrush Current Calculation for Example Capacitor Bank**

Assume the fault is at the line side bushings of a line breaker since that will give the highest peak current because it will have the lowest inductance. The circuit distance is 60' + 52' (bay width) +50' to the capacitor bank for a length of 162' corresponding to the following inductance:

\[ L = 0.3 \mu H / ft \times 162 \text{ ft} + 10 \mu H = 58.6 \mu H \]  

(28)

For the initial bank, the rating = 82 Mvar at 230 kV

\[ C_{\text{initial}} = \frac{82 \times 10^6}{377 \times 230^2} = 4.1 \mu F \]  

(29)

The maximum (future) bank rating 205 Mvar at 230 kV

\[ C_{\text{max}} = \frac{204 \times 10^6}{377 \times 230^2} = 10.3 \mu F \]  

(30)

Therefore, the outrush current peak and frequency for the initial and maximum rated capacitor bank sizes are as follows:

\[ I_{\text{initial}} = 230 \times \sqrt{\frac{2}{3}} \times \sqrt{\frac{4.1}{58.6}} = 49.7 kA \]  

(31)

\[ f_{\text{initial}} = \frac{1}{2\pi \sqrt{58.6 \times 10^{-6} \times 4.1 \times 10^{-6}}} = 10 kHz \]  

(32)

\[ I_{\text{max}} = 230 \times \sqrt{\frac{2}{3}} \times \sqrt{\frac{10.3}{58.6}} = 78.7 kA \]  

(33)
\[ f_{\text{max}} = \frac{1}{2\pi \sqrt{58.6 \times 10^{-6} \times 10.3 \times 10^{-6}}} = 6.5 \text{kHz} \]  

(34)

Since 78.7 kA < 163.8 kA, no TLI is required.

Even allowing for a reignition outrush 78.7 kA < 81.9 kA (163.8/2)

One needs to remember that although there will not be damage to the circuit breaker from outrush, there are possible protection and control system concerns. The outrush current will generate transient ground rise between the capacitor bank and the point of fault. While the chosen fault location produces the largest outrush current, which is important for the circuit breakers, another location, perhaps on the other side of the control cubicle could produce worse control system transients. Current circuits are normally grounded in the control cubicle. This remote ground is present on the CT cores and on the CT terminal blocks at the line breakers. During an outrush event, there will be a significant potential difference (many kV) between the CT star point at the circuit breaker, and the Control cubicle ground. Placing a 20mm diameter 1000 V MOV from the CT star point to local ground will safely clamp that potential difference. If high impedance relays are used for bus differential, then MOVs (1000 V 20 mm diameter) should be placed across the CT windings. [MOV voltage ratings can be determined using the standard insulation coordination procedures. The voltage rating is straight forward. Energy calculations are quite complex. The above ratings have been used successfully for more than 20 years.]

All CT secondaries on the capacitor bank should be protected with MOVs on their terminals.

Also the high di/dt from an outrush will produce common mode voltages on any unshielded control or power cables near the outrush, or outrush return, path.

Oil breakers have limits on closing, when initiating a capacitive discharge, both on the peak current and the frequency. Vacuum and SF\(_6\) breakers have limits on closing outrush current magnitude. Details of this limitation will be discussed in the Appendix D “Capacitor Bank TLI Sizing and Application Guide Including TRV Mitigation”.
APPENDIX D

Capacitor Bank TLI Sizing and Application Guide Including TRV Mitigation

D.1 Terminology

The inductor placed in series with an isolated (single) capacitor bank is usually installed to control the magnitude of outrush current from the capacitor bank to a breaker closing into a fault. Often, as in the case of the example in Appendix C, this is a line breaker closing into a close in fault on its terminals. These inductors are referred to as “Transient Limiting Inductors (TLI)” This is the Capacitor Subcommittee’s choice.

“Transient Recovery Voltage (TRV)” this is the circuit response to a current interruption at a naturally occurring current zero.

“Initial Transient Recovery Voltage (ITRV)” is the fast traveling wave component of TRV at a Bus see IEEE C37.04 1999 clause 5.9.2.3

“Short Line Fault (SLF) TRV” is sawtooth traveling wave TRV which results from a fault on a roughly 1km line length. It is defined in terms of percentage of the terminal fault current rating as decreased by a short line segment. See IEEE C37.04-1999 5.9.2.2

“Fast TRV” is a 1-cosine wave shape TRV from an inductor or Transformer limited fault. See IEEE C37.06.1-2000 where a fast TRV is demonstrated by a special test which has a maximum steepness about 5 times the “normal” 30% terminal fault requirement.

Information needed to conduct study:

- Short-circuit duty to be used. i.e., actual short-circuit levels now and future, or design base short-circuit level.
- Voltage rating
- Initial and ultimate capacitor bank size, Mvar
- Circuit breaker ratings/capabilities of line, tie, transformer breakers in the station
  - Interruption technology (SF₆, vacuum, oil, air blast )
  - Terminal fault rating, if used for breaker failure of capacitor protection breaker
  - SLF capability with no added OR INTERNAL capacitance (90%SLF)
  - ITRV capability with no added or internal capacitance
  - Does breaker pass Fast TRV requirements of C37.06.1-2007?
- Capacitor protection breaker ratings/capabilities
  - Terminal fault rating
  - SLF capability with no added OR INTERNAL capacitance (90%SLF)
– ITRV capability with no added or internal capacitance
– Does breaker pass Fast TRV requirements of C37.06.1-2007?

• Station Layout
• Is there a desire to make the cap bank a harmonic filter?
• How transient hardened is the protection/control system?
• Is it better to transient harden the control/protection system (i.e. install MOVs where needed) or reduce the severity (di/dt) of outrush and back to back transients?
• Risk aversion to rare fault events as outrush, and total cap bank fault.
• For back to back cases, how often will the capacitors be switched back to back?
  – What contact life is desired?
  – What is the back to back wear limit (cumulative I x t) for the capacitor switching device?

D.2 Introduction

In the Case in Appendix C (230 kV Capacitor Bank), it was found that outrush limiting TLIs (damping reactors) are not required to protect the Circuit Breakers. If Vacuum Breakers or Oil breakers were on the bus, the situation would have been different.

Switchgear Concerns on capacitor switching:

• Frequent switching. Capacitors are often switched daily. A typical transmission breaker may switch a few times per year and interrupt short-circuits a few times per year. Capacitor switching devices, in general, see several orders of magnitude more operations in its life than line breakers. Typical expectation is 10,000 operations in a 40 year life for capacitor switching, compared to 200 operations in the same 40 year life for a line, transformer, or bus section breaker.
• Inrush currents during switching, particularly back to back switching. This is a frequent event perhaps 10,000 operations in 40 years. Back to back switching can be particularly onerous. Back to back inrush frequencies range from 2 – 20 kHz depending on the specifics. The multi-kHz transient arc tends to be more compact than a 60 Hz arc. The burning on the contacts is more localized, and can make for dielectric stress enhancements when the contacts are open. It has been observed that for pin and tulip style contacts, contact erosion tends to make the pin contact conical. The cumulative I x t during the time of the closing arc will determine the degree of contact erosion. Keeping inrush current cumulative I x t below manufacturer’s recommendations will promote long contact life.
• Outrush current when closing into a fault has a higher magnitude and a similar frequency as back to back inrush currents. The big difference is that outrush from closing into a fault is expected to be a rare event, occurring only
a few times (if ever) in a circuit breaker’s 40 year life. Outrush can possibly affect all line, transformer, and tie breakers in a station. It does not affect the capacitor switching breaker (or switch).

Capacitor switching inrush currents can be controlled with: Controlled Switching; Pre-insertion resistors, and pre-insertion inductors. Fixed TLIs (damping reactors or CLRs) can also be used to limit inrush transient currents, but are less effective than controlled switching or properly sized pre-insertion impedances.

Outrush is another matter. Controlled switching is not reasonable to apply to an infrequently operated line breaker. Closing resistors either are not available on some breakers, or not sized properly to control outrush. The only practical control of outrush current magnitudes is with TLIs (Damping Reactors). Tuning Inductors for a harmonic filter will also be effective in limiting outrush currents.

For SF₆ breakers, the inherent self inductance of buswork and leads will usually be enough to keep outrush currents within their capabilities, since they can withstand quite large outrush currents without damage.

Vacuum breakers may suffer from serious contact welding if the outrush current is too high. Serious welding in its most severe form will prevent opening of the contacts by the driving mechanism. At lower currents, welds breakable by the driving mechanism may produce stress enhancements on the contacts, or result in particles sloughing off, either of these can lead to restriking on subsequent operations. This may be unacceptable for capacitor, unloaded line, or cable switching. In other applications, restrikes may be less of a concern. Often, numerous live switching operations will burn off the offending stress enhancement, or vaporize the free particles.

Oil Circuit Breakers can suffer shock wave damage to the interrupter if the product of the peak current and the frequency is too high (I x f is too large). The result is destruction of the interrupting chamber and loss of fault interrupting capability.

D.3 Proposed method for determining Capacitive Inrush (outrush) capability of circuit breakers

In no case should the Inrush/outrush current exceed 2.6 x the rms short-circuit rating of the breaker (i.e. close and latch peak current).

For the shock wave portion, based on the prestrike arc shock wave theory:

\[ I \times f = k \]  \hspace{1cm} (35)

Where:

- \( I \) = allowable peak current (expressed in same units as short-circuit rating)
- \( f \) = the natural frequency of the circuit (kHz)
k = a constant different for each major interruption technology (and different for each interrupter design)

For bulk oil breakers: k=85 kAkHz

For SF₆ breakers: k= 2500 kAkHz

For Vacuum breakers wishing to attain Class C₂ I<7kA regardless of frequency

For Vacuum breakers wishing to attain class C₁ I<20kA regardless of frequency

Based on these proposed limits, the minimum inductance (L) required would be calculated as follows:

\[ L = \frac{V_{\text{peak}}}{2\pi k} \]  \hspace{1cm} (36)

One can see that the required minimum L is independent of C. It should be understood that there is some minimum threshold energy, below which shock wave damage will not occur. While we don’t know precisely what this energy is, experience has shown that capacitance in the few nF range does not seem to provide enough energy to cause shock wave damage.

Equation (36) is only concerned with the shock wave portion of the discharge energy, much of the energy available from the capacitive circuit is dissipated in the circuit resistance (buswork leads and the series resistance of the capacitor bank itself). Another small portion goes into contact ablation (erosion of the breaker contacts). It is this portion that may be the limiting feature for SF₆ breakers switching back to back capacitors. Each breaker design will have a limit on the accumulated I x t during the time that a closing arc is burning during back to back switching that will give acceptable contact life and switching performance. The manufacturer should be consulted to tell what this limit is.

For outrush, parametric analysis for SF₆ breakers, leads to the conclusion that only a few 10s of microhenries will be required in most cases, since SF₆ is not very sensitive to shock waves. That minimum inductance will usually be satisfied by the natural bank and bus inductance.

**D.4 Vacuum Breaker Example**

Vacuum Breakers as of 2011 are available at voltage ratings up to 145 kV in a single interrupter.

Let’s assume we want to keep the peak current below 20 kA on an outrush current and we don’t care about the frequency.

We have:
\[ I_{\text{peak}} = V_{\text{peak}} \sqrt{\frac{C}{L}} = 0.816xV_{\text{L-L}} \sqrt{\frac{C}{L}} \]  

(37)

and

\[ C = \frac{\text{Var}}{\omega V^2} \]  

(38)

Where:

\[ C = \text{capacitance in microfarads} \]
\[ V = \text{rms kV} \]
\[ L = \text{inductance in micro henries} \]

Note: If Var is three-phase, V is line to line kV
If Var is single phase, V is line to ground kV

Combining and using \( V_{\text{L-L}} \):

\[ I_{\text{peak}} = 0.816xV_{\text{L-L}} \sqrt{\frac{\text{Var}}{\omega V^2 L}} \]  

(39)

Solving for \( L \):

\[ L = \frac{0.6659 \times \text{Var}}{\omega \times I_{\text{peak}}^2} = 0.001766 \times \frac{\text{Var}}{I_{\text{peak}}^2} \]  

(40)

Notice how this inductance value is independent of Voltage, and only depends on the capacitor Mvar rating.

To keep \( I_{\text{peak}} \) below 20 kA with 28.8 Mvar capacitor bank, an \( L \) of 128 \( \mu \)H or greater is required. To keep \( I_{\text{peak}} \) below 7 kA a larger inductor would be required by a factor of \((20/7)^2\), giving a required inductance of 1.05 mH.

TRV mitigation for a capacitor bank short will not be considered in this example. If the capacitor protection breaker is SF\(_6\), the methodology is the same as for the 630 \( \mu \)H example under “Line Oil Breaker Example” below. The capacitor will have a slightly different capacitance. If the capacitor protection breaker is a vacuum breaker, the fast TRV will be easy for it, and no TRV mitigation may be required.

**D.5 Line Oil Breaker Example and TRV Calculations**

Let’s assume we had a 50 kA oil breaker that you wanted to protect from outrush damage.
Assume it was determined that the minimum \( L = 688 \, \mu\text{H} \) and there is \( 58 \, \mu\text{H} \) of natural buswork inductance, so the additional inductance required is \( 688-58 = 630 \, \mu\text{H} \).

Current ratings for the TLI

Continuous Current:

The minimum continuous current rating should be \( 1.4 \times \) the maximum continuous 60 Hz current of the capacitor bank calculated as follows for a 230 kV 205 Mvar capacitor bank:

\[
I_{\text{continuous}} = 1.4 \times \frac{\text{Var}}{\sqrt{3} \times V} = 1.4 \times \frac{205 \times 10^6}{\sqrt{3} \times 230 \times 10^3} = 720 \text{A} \quad \text{(rounded to 800A)} \quad (41)
\]

Short-Circuit Rating:

For a small inductance inductor, the peak current short-circuit rating must equal or exceed the maximum expected peak current short-circuit duty at the substation. Usually a minimum of a 1.25 safety factor is applied.

Potential TRV Concern

\( \text{SF}_6 \) breakers have a characteristic low capability to withstand Fast/Steep Transient Recovery Voltages. This includes short line fault and inductive faults. If a fixed inductor is more than 1\% of the fault impedance, an \( \text{SF}_6 \) breaker may have trouble with it. The first few microseconds of TRV are very difficult for an \( \text{SF}_6 \) breaker to withstand. Oil and Vacuum breakers do not have this characteristic.

The TLI is placed in series with the capacitor bank, to limit the outrush current. If a fault develops shorting out the Capacitor bank, the TLI may comprise more than 1\% of the fault impedance and may cause the breaker TRV trouble. This is true whether the TLI is placed at the line end or neutral end of the capacitor. An analysis needs to be done to check if the TLI can cause an excessive TRV for \( \text{SF}_6 \) circuit breakers.

In this example, the short-circuit current is 19.4 kA three-phase and 15.7 kA phase to ground.

The worst case is generally the greater short-circuit current, but it is unlikely to have a three-phase short of each capacitor phase simultaneously for this example.

However, we will calculate phase to ground equivalent inductances for both the single line to ground and three-phase fault currents for this example.

\[
L_{\text{sourceG}} = \frac{V}{\sqrt{3} \times I \times \omega} = \frac{230 \times 10^3}{\sqrt{3} \times 15.7 \times 10^3 \times 377} = 22.4 \, \text{mH} \quad (42)
\]
The next step is to calculate what proportion of voltage will remain on the TLI during a capacitor fault.

For a good (low loss) inductor, the TRV peak will be 1.8 x the peak voltage during the fault. (damping factor =0.81) the TRV voltage is a 1-cosine and will start at zero, and ½ cycle of TRV frequency later, be at the first peak voltage.

For 230 kV use 245 kV x .816 = 200 kVpeak.

For the single phase fault:

\[ V = \frac{L_{TLI}}{L_{TLI} + L_{sourceG}} x V_{peak} x 1.8 = \frac{630 \times 10^{-6}}{630 \times 10^{-6} + 22.4 \times 10^{-3}} \times 200 \times 1.8 = 10 \text{kV} \]  

(44)

For the three-phase fault:

\[ V = \frac{L_{TLI}}{L_{TLI} + L_{source3}} x V_{peak} x 1.8 = \frac{630 \times 10^{-6}}{630 \times 10^{-6} + 18.2 \times 10^{-3}} \times 200 \times 1.8 = 12 \text{kV} \]  

(45)

The natural frequency of an air core TLI coil and the connections will be about 700 kHz (from experience) which means the first peak of the TRV occurring in ½ cycle will be in 0.7 µs.

What is the breaker TRV Capability for this condition?

The ITRV capability is 4.25 kV in 0.6 µs. (not high enough). The SLF capability based on 90% SLF at 45 kA and no added capacitance is 10.8 kV/µs after a 0.5 µs delay. In this example the breakers are stressed to less than ½ of their no capacitance SLF capability, and they are “pure” puffers, they may withstand these onerous TRVs, especially in the single line to ground case. Note: this method is not applicable to self blast or arc assist interrupters.

So, you may get away with no TRV mitigation. However, without test data, this is a poorly defendable position.

Determine size of TRV Mitigation Capacitor

Determine target TRV Frequency

Since a 630 µH inductor will have a relatively small proportion of fault voltage across it, the 90% SLF TRV capability can be used. A 0.5 µs time delay roughly equates to 30 degrees after the trough of a TRV sine wave. Consider a trapezoidal wave starting at zero, then after 0.5 µs begins a 10.8 kV/µs rise for 2 µs, then is
constant for 1 µs, then heads back down to zero. Thus the period of the wave would be 360/30 (12) x 0.5 µs = 6 µs. The SLF equivalent TRV frequency is thus 166 kHz.

Where does the 10.8 kV/µs come from? The short line fault TRV is a ramp. The slope of the current is the di/dt of 60 Hz at zero (where the current is extinguished). The voltage is simply this slope x the assumed surge impedance of 450 ohms. The unassisted 90% SLF TRV capability is 50 kA. That means the actual current is 90% of 50 kA = 45 kA so the TRV slope is $\sqrt{2} \times 45 \text{ kA} \times 377/s \times 450 \text{ ohm} = 10.8 \times 10^6 \text{ kV/second} = 10.8 \text{kV/µs}$

The equivalent peak to peak amplitude converting a trapezoidal wave to a sine wave will be $2 \times \frac{10.8 \text{ kV}}{\mu s} \times 2/\sqrt{3} = 24.8 \text{ kV}$. Our TLI peak to peak voltage is 12 kV. The 90% SLF TRV first peak = $200 \text{ kV} \times 1.6 \times (1-0.9) = 32 \text{ kV}$ so we are OK on peak TRV capability (32 kV>12 kV). Therefore the peak voltage is not a concern. Since our amplitude is decreased by a factor of $12/24.8=0.5$. The target frequency can be increased by $\sqrt{1/0.5} = 1.4$. So our target TRV frequency is $1.4 \times 166 \text{ kHz} = 232 \text{ kHz}$.

What capacitance in parallel with 630 µH will give a frequency of 232 kHz? The following shows the calculation of the minimum required capacitance:

$$C = \frac{1}{\left( \frac{1}{2\pi f} \right)^2 L} \quad \text{(46)}$$

Where:

- $f$ in MHz
- $C$ in µF
- $L$ in µH

Inserting values for this example:

$$C = \frac{1}{\left( \frac{1}{2\pi \times 0.23} \right)^2 \times 630} = 747 \text{ pF} \quad \text{(47)}$$

It doesn't hurt to go larger on the capacitance. For example, a 3750 pF 230kV capacitor (which is a reasonable size for a 230 kV CCVT) would work for this example.

Insulation Level

How do we choose the voltage rating? Both of these devices will only see significant voltage during a capacitor outrush and other high frequency transients such as lightning. On fast transients, the TLI would be expected to flash over before failing turn to turn. It basically needs to support voltage across itself during the outrush condition. It only requires a BIL of about 2.2 x Peak phase to ground voltage, or for a
230 kV application, 450 kV. In specifying the TLI insulation level mention that it is expected to flash over externally before failing turn to turn, for a 1.2 x 50 µs Impulse (standard BIL waveform). The TRV shaping capacitor, in effect, could be protected by the coil flashing over, but this is not a truly coordinated system, we don’t know what the coil flashover will be. The 230 kV system has no line entrance arresters however there will be nodal reflections of external lightning transients coming in on a line. With one line out of service, and 1 line coming into 2, the voltage would be 2/3 of the incoming transient voltage. Or 2/3 x 1300 kV = 858 kV. For this application, it is recommended that the TRV shaping capacitor have a BIL at least to the 900 kV BIL station insulation. In a case with many 230 kV lines, the insulation level could be lower.

So:

- TLI BIL minimum 450 kV [an Arrester across the TLI may be advisable to protect for lightning transients.]
- TRV shaping capacitor BIL minimum 900 kV

The foregoing is based on the maximum Capacitor bank size.

Analyze based on the numbers above k = 85 V = 200kV (Using equation 36)

\[
L = \frac{V_{\text{peak}}}{2\pi k}
\]

(48)

\[
L = \left( \frac{V_{l} - g}{6.28x85} \right) = \left( \frac{200}{533.8} \right) = 375 \mu H
\]

(49)

From the example capacitor, the inductance to the fault is about 58 µH so the additional inductance required is 375-58 = 317 µH.

The short-circuit and mechanical peak current ratings are the same as for the 630 µH inductor.

TRV Concern with Smaller inductor.

The first peak of fast TRV will be reduced by a factor of 317/630 = 0.5 since this approach is less conservative, we will use the line to ground fault inductance. The first peak will be .5 x 10 = 5 kV. This is still more than the ITRV peak, so that capability cannot be used. We are stuck with the unassisted 90% SLF TRV. If we assume that the self capacitance of the inductor and leads is the same as the 630 µH inductor, the frequency will go up as \( \sqrt{630/317} = 1.4 \). The assumed frequency of the 630 µH inductor was 700 kHz, the 317 µH inductor will give a TRV frequency of 1.4 x 700 = 980 kHz. Using the same analysis as above to attain the target natural
frequency of the TLI in parallel with a TRV shaping capacitor, we get Target \( f = \sqrt{\frac{28.4}{5}} \times 166 \text{ kHz} = 395 \text{ kHz} \).

As above:

\[
C = \frac{1}{(2\pi f)^2 L} = \frac{1}{(2\pi \times 395)^2 317} = 504 \text{ pF}
\]  \hspace{1cm} (50)

This is smaller than for the 630 \( \mu \text{H} \) inductor. The voltage rating concerns are identical and thus unchanged.

However, as discussed above, the SLF TRV capability is based on a 45 kA fault and here we have just about 1/3 of that. The SLF TRV capability of a pure puffer (no arc assist) will undoubtedly be higher. It might be high enough that no parallel capacitor is required. One could assume that the 0.5 \( \mu \text{s} \) SLF TRV delay at 45 kA could easily drop to 0.15 \( \mu \text{s} \) at 16 kA, and the TRV steepness could be much higher. In my judgment the likelihood of “getting by” with no TRV shaping capacitor is about 85 - 15 in this case.

On a risk basis, the likelihood of a fault of the entire capacitor bank is small, so that one might just take the risk. However, NERC is aware of this phenomenon after a TRV failure to interrupt after a Hydro One 230 kV Capacitor bank phase to phase fault, and issued an alert to all utilities. If such a failure occurred, one would be “without excuse” at the NERC hearings, and the utility could be fined. The seriousness would depend on the system consequences.

Harmonic Filter

The above treatment arrived at the minimum inductor size for the TLI (damping reactor) to protect circuit breakers from outrush damage. There are reasons other than switchgear limitations, why a larger Inductor might be used.

My thinking in these situations was: “If I have to install an inductor and TRV mitigation capacitor, it may as well do something useful”.

- A larger inductor will reduce the \( di/dt \) of the outrush, which would lower transient ground rise, and lower the induced voltages on control cables.
- It would also lower the frequency and amplitude of the normal energizing transient currents. Whether the change in frequency is a good or bad thing depends on the details of any downstream voltage magnification issues.
- There is some 5th, 7th, 11th, and 13th harmonic in the system voltage that could be shunted with a harmonic filter. One can easily tune the Capacitor to become a harmonic filter branch. Choosing the tuning frequency should be done with a harmonic study, so the most offending harmonic can be filtered. Future increase of the capacitor bank size will lower the tuning frequency, unless new inductors are purchased at that time. Lower order harmonic
filters will increase the voltage rating needs of the capacitor bank. The guidance in IEEE 1531 [3] should be followed.

Reducing Outrush $\frac{di}{dt}$

If one wished to reduce the outrush $\frac{di}{dt}$ to protect the control system, what would be a reasonable value?

How about the 60 Hz design short-circuit $\frac{di}{dt}$? An example for a 63 kA short-circuit current is shown below:

$$\frac{di}{dt} = \sqrt{2} \times 63\text{kA} \times 2\pi \times 60\text{Hz} = 33553\text{kA/s} = 3.36 \times 10^7 \text{A/s}$$  \hspace{1cm} (51)

If we look at our series RLC formulas and forget the R:

$$I = \frac{V}{\sqrt{L/C}}, \quad \omega = \frac{1}{\sqrt{LC}}, \quad \text{and} \quad \frac{di}{dt} = \omega I$$  \hspace{1cm} (52)

$$\frac{di}{dt} = \omega I = 3.36 \times 10^7 = \frac{1}{\sqrt{LC}} \times V_{\text{peak}} \sqrt{\frac{C}{L}}$$  \hspace{1cm} (53)

Solving for $L$:

$$L = \frac{V_{\text{peak}}}{3.36 \times 10^7} = \frac{200 \times 10^3}{3.36 \times 10^7} = 5.9 \text{ mH (rounded to 6 mH)}$$  \hspace{1cm} (54)

What is the natural frequency?

$$f = \frac{1}{2\pi \sqrt{LC}} = \frac{1}{2\pi \sqrt{6 \times 10^{-3} \times 4.1 \times 10^{-6}}} = 1 \text{ kHz}$$  \hspace{1cm} (55)

That is too high to catch any of the prevalent harmonics. $1000/60 = 16.7^{\text{th}}$ Harmonic. If we were to target $11^{\text{th}}$ harmonic:

$11^{\text{th}}$ (future 7) Harmonic filter

$L = (16.7/11)^2 \times 6 \text{ mH} = 13.8 \text{ mH}$. Actually one would detune to the low side a little (say 3%) so the inductance would be increased by $(1.03)^2$ to 14.6 mH

For example, let’s choose 14.5 mH. Now we no longer have a TLI (Damping reactor) but a Filter Inductor.

Continuous current is the same as the TLI or 800 A. If you keep the 14.5 mH inductor and max-out the bank to 204 Mvar, the natural frequency drops by $\sqrt{(82/204)} \times 0.63$ and voila! You have a 7th harmonic filter!
The short-circuit current rating can be a little less because the inductor will significantly reduce the short-circuit current. In fact, the reduction is the same as the per unit voltage across the coil during a short-circuit, i.e., 40% reduction (see below). So the rated short-circuit can be 15 kA for the 14.5 mH inductor.

The mechanical peak is still \(2.82 \times \text{short-circuit} = 42.3\ \text{kA}\)

Check TRV Concerns

Now a substantial portion of the fault voltage will be dropped across the inductor. For the single phase fault case, the proportion of the fault voltage across the inductor will be \(14.5/(14.5 + 22.4) = 0.393\). As before, we need to calculate a target frequency for the allowable TRV so we can size the TRV shaping capacitor. With such a high TRV voltage, it no longer makes sense to use the SLF TRV. We will assume the breakers all passed the C37.06.1 tests for fast TRV.

From Table 3B of C37.06.1-2000 for a 245 kV 63 kA breaker we read for currents 19 kA and below, the Fast TRV has a peak voltage of 487 kV and a time to peak of 30.3 \(\mu\)s. This is a 1-cos TRV so it starts at zero and \(\frac{1}{2}\) cycle later is at a peak of 487 kV. We need the full cycle parameters to use this to get to a target TRV frequency. Thus the amplitude is 487 kV/2 = 243.5 kV. The period is 30.3 \(\times\) 2 = 60.6 \(\mu\)s. The frequency is then \(1/60.6\ \mu\)s = .0165 MHz = 16.5 kHz. For our inductor, the peak fault voltage is 200 kV \(\times\) 0.4 = 80 kV. As before, the target TRV frequency is (243.5/80)\(1/2\) \(\times\) 16.5 kHz = 28.8 kHz. The natural frequency of a 14.5 mH inductor is about 150 kHz, therefore we will need added capacitance.

As before:

\[
C = \frac{1}{(2\pi f)^2 L} = \frac{1}{(2\pi \times 28800)^2 \times 0.0145} = 2.1\ \text{nF}
\]  

The voltage ratings of the tuning inductor and TRV mitigation capacitor are the same as for the TLI and its mitigation capacitor:

Tuning inductor 450 kV BIL (minimum)

TRV Mitigation capacitor 900 kV BIL (minimum)

Physical Mounting of the Inductor and TRV mitigation Capacitor

For banks 230kV and below, the most convenient mounting of the inductor and its parallel TRV mitigation capacitor is on top of the capacitor rack structure. The capacitor rack and insulators need to be designed to support the weight and wind loading of these devices.