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IEEE Electronics Packaging Society (EPS) - Phoenix Chapter

Formerly Known as Components, Packaging and Manufacturing Technology (CPMT) Society

Remember this meeting is on Monday, October 16, 2017, 5:30 PM

System in Package (SiP) Packaging Technology Trends

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ABSTRACT

System-in-package (SiP) technology has been evolving through utilization of various package technology building blocks to serve the market needs with respect to miniaturization, higher integration, and smaller form factor, with the added benefits of lower cost and faster time to market as compared to silicon (Si) level integration, which is commonly called SoC or system-on-chip. As such, SiP incorporates flip-chip (FC), wire bond (WB), and wafer-level packaging (WLP) as its technology building blocks, and serves various end applications in all markets. Several key technologies are available as viable alternatives to the traditional SiP using a laminate type of solutions. Advanced embedded Wafer Level Ball Grid Array (eWLB) technology provides a versatile platform for the semiconductor industry's technology evolution from single or multi-die 2D package designs to 2.5D interposers and 3D System-in-Package (SiP) configurations. Molded Interconnect Substrate (MIS) is another technology that can enable integration while managing lower costs. This presentation will review the packaging technology advancements in SiP as well as new packaging technologies for SiP.

BIOGRAPHY

Vinayak Pandey, VP
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Vinayak Pandey is the Vice President of Product & Technology Marketing at STATS ChipPAC where he is responsible for driving advanced packaging and SiP marketing and business development in the US region. Vinayak has more than 10 years of experience in business development, marketing and product line management to support customers in a wide range of semiconductor markets. Prior to STATS ChipPAC, Vinayak worked several years at Intel Corporation in microprocessor packaging. He has an MBA from Arizona State University and a Master of Science degree in Engineering Mechanics from Virginia Tech.

Date: **Monday, October 16, 2017, 5:30 PM**

Location: **Meeting Room B**
Tempe Public Library
3500 S. Rural Road, Tempe, AZ 85282
(S-W corner of Rural & Southern Ave.)
https://www.google.com/maps/dir/''/tempe+library/

Agenda: 5:30–6:00 PM: Networking & Refreshments,
6:00–7:00 PM: Presentation,
7:00 – 7:30 PM Questions & Answers
(Snacks and Soda will be provided by the IEEE Phoenix Section, EP Society Chapter)
IEEE members and non-members are all welcome to attend. The presentation promptly starts at 6:00 PM.

For more information, please contact any of the following EPS officers:

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