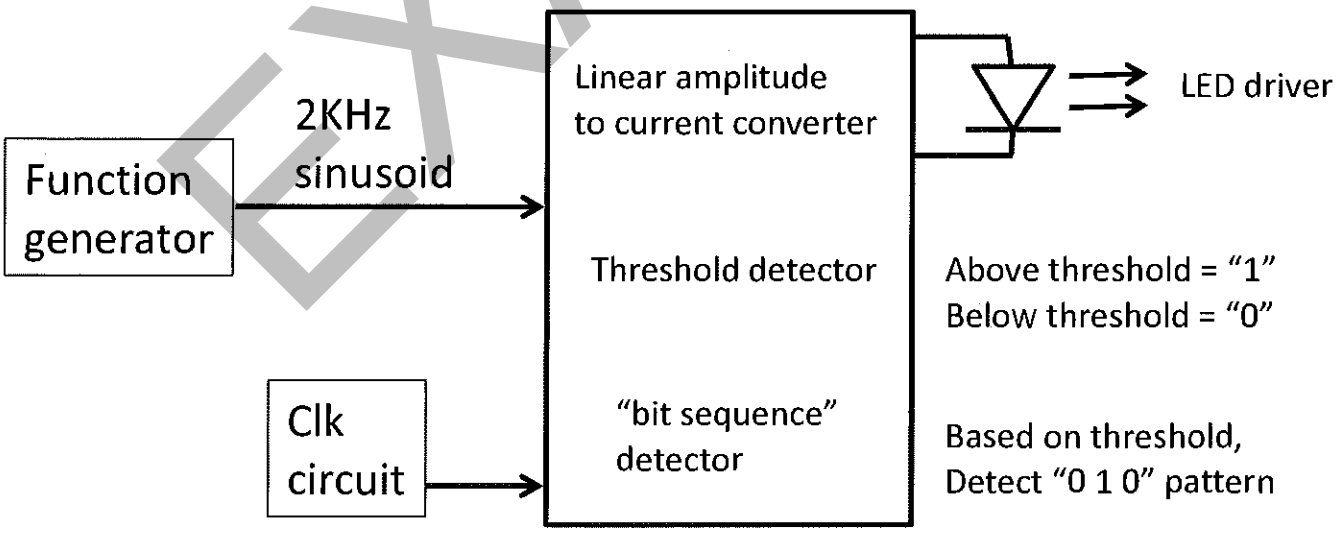
IEEE Student Design Competition 2015

Circuit Requirements/Description

The circuit to be designed will detect the amplitude of an incoming sinusoid and linearly drive the current through an LED in proportion to the amplitude of the incoming sinusoid. In parallel with this capability, the circuit shall detect when the amplitude is above a given threshold, which will be considered a logical "1" and when the amplitude is below a given threshold, which will be considered a logical "0". When the amplitude of the input sinusoid is varied with respect to time to create a "0 1 0" sequence, the circuitry will detect the sequence and provide a logical "1" for this condition.

1. The circuit shall have an input capable of receiving an analog signal comprising a sinusoid with a max amplitude of +/-2volts.
2. The frequency of the sinusoid shall be 2 KHz.
3. The amplitude of the input sinusoid shall vary from +/-1volts to +/- 2 volts.
4. The circuit shall linearly detect the amplitude of the sinusoid as it varies from +/- 1 volts to +/- 2 volts. Using this detected amplitude (voltage), the circuit shall provide a current drive that linearly tracks the detected amplitude according to the following boundary conditions and accuracy:
    a. Sinusoid peak = +/- 1 volts the current drive shall supply 5 to 7 milliamps
    b. When the sinusoid peak = +/- 2 volts, the current drive shall supply 10 to 13 milliamps
5. The current drive shall light an LED. Therefore, the LED intensity should change in "brightness" as the amplitude of the sinusoid is varied.
6. In parallel with the current drive, the circuit shall detect when the amplitude of the sinusoid exceeds +/- 1.5 volts and generate a logical "1" for this condition. When the amplitude is below +/- 1.5 volts, the circuit will generate a logical "0" for this condition.
7. As an additional requirement, a clock circuit shall be built with a frequency of 0.5 to 1 Hz.
8. When the amplitude of the sinusoid is manually varied close to the frequency of the clock, a sequence of "0 1 0" shall be detectable using the criteria of #6 above.



Circuit elements provided:

1. Various resistors
2. Various capacitors
3. TL082 dual op amps
4. 741 op amps
5. LM393 comparators
6. MC74HC175 Quad D type FF
7. SN54HCT32 OR logic gates
8. SN54HC14 Hex Schmitt-Trigger Inverters
9. SN7408 2 input AND logic gates
10. LEDs
11. Breadboard, wires, etc.

TL08xx JFET-Input Operational Amplifiers

Check for Samples: TL081, TL081A, TL081B, TL082, TL082A, TL082B, TL084, TL084A, TL084B

FEATURES

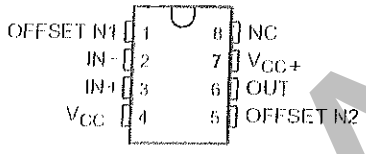
- Low Power Consumption: 1.4 mA/ch Typ
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias Current: 30 pA Typ
- Low Input Offset Current: 5 pA Typ
- Output Short-Circuit Protection
- Low Total Harmonic Distortion: 0.003% Typ
- High Input Impedance: JFET Input Stage
- Latch-Up-Free Operation
- High Slew Rate: 13 V/μs Typ
- Common-Mode Input Voltage Range Includes V_{CC+}

DESCRIPTION

The TL08xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

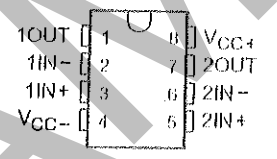
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The Q-suffix devices are characterized for operation from −40°C to 125°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

TL081, TL081A, TL081B
D, P, OR PS PACKAGE
(TOP VIEW)

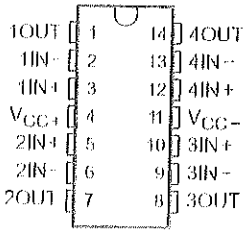


NC – No internal connection

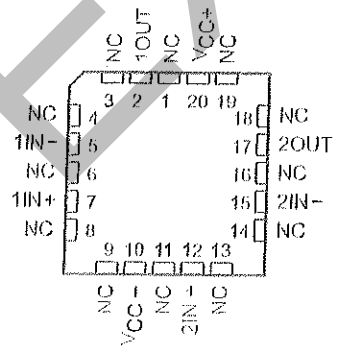
TL082, TL082A, TL082B
D, JG, P, PS, OR PW PACKAGE
(TOP VIEW)



TL084, TL084A, TL084B
D, J, N, NS, OR PW PACKAGE
(TOP VIEW)

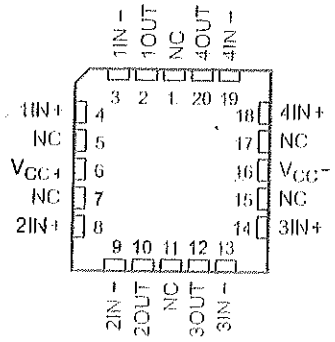


TL082M . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

TL084M . . . FK PACKAGE
(TOP VIEW)

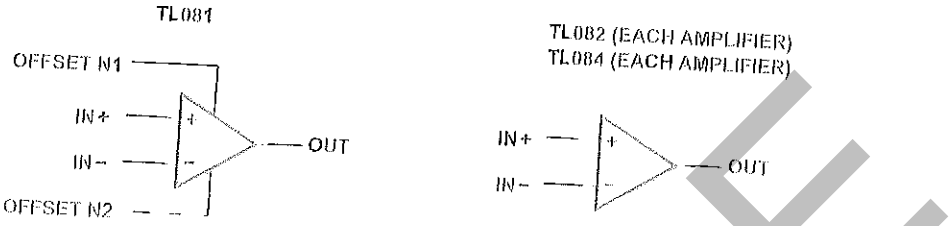


NC – No internal connection

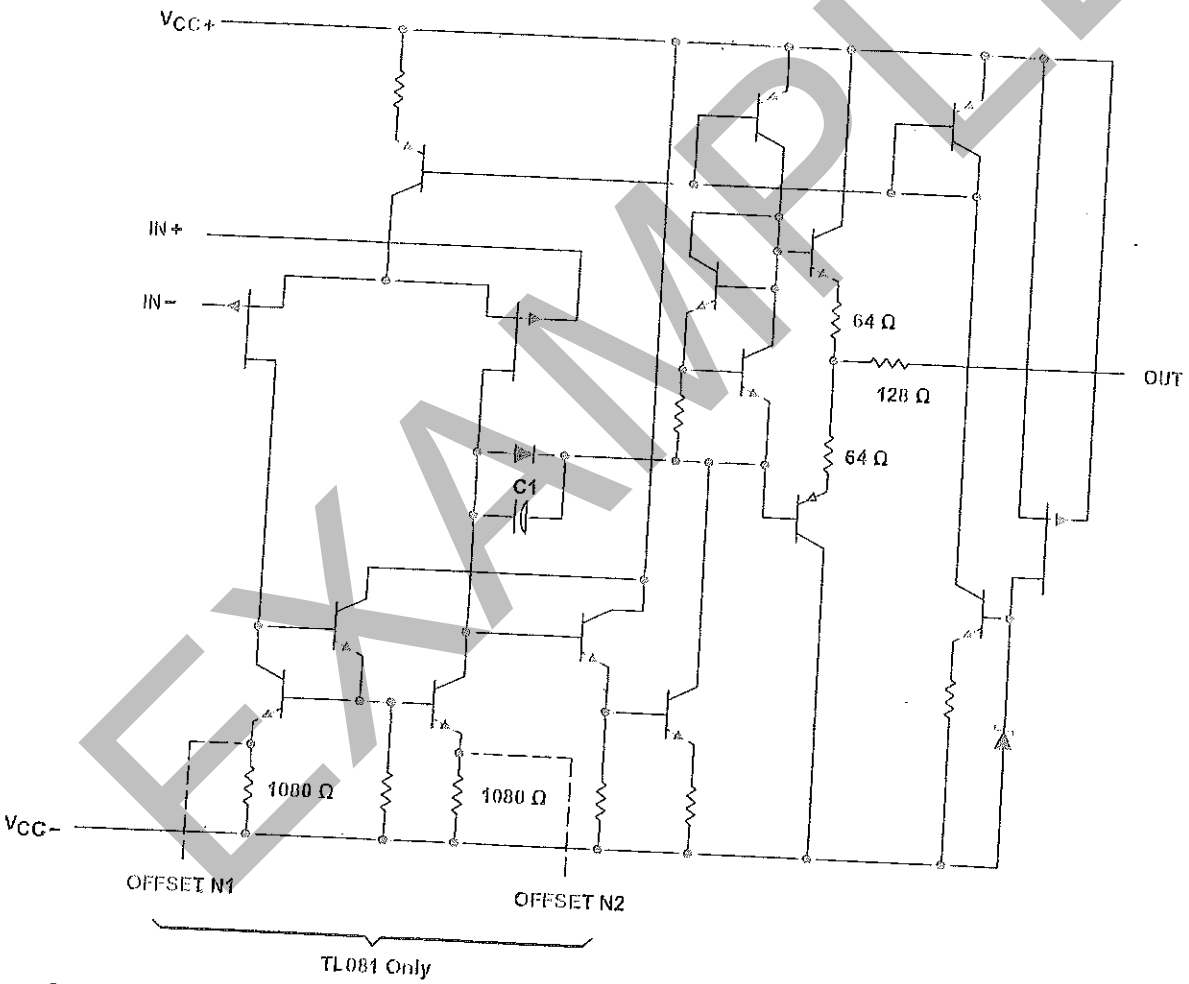
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Symbols



Schematic (Each Amplifier)



Component values shown are nominal.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			TL08_C TL08_AC TL08_BC	TL08_I	TL084Q	TL08_M	UNIT
V_{CC+} / V_{CC-}	Supply voltage(2)		18	18	18	18	V
V_{ID}	Differential input voltage(3)		−18	−18	−18	−18	
V_I	Input voltage(2)(4)		±30	±30	±30	±30	V
	Duration of output short circuit(5)		±15	±15	±15	±15	V
	Continuous total power dissipation		Unlimited	Unlimited	Unlimited	Unlimited	
T_A	Operating free-air temperature range		See Dissipation Rating Table				
θ_{JA}	Package thermal impedance(6)(7)	D package (8-pin)	0 to 70	−40 to 85	−40 to 125	−55 to 125	°C
		D package (14-pin)	97	97		97	°C/W
		N package (14-pin)	86	86		86	
		NS package (14-pin)	76	76		80	
		P package	80			76	
		PS package	85	85		85	
		PW package (8 pin)	95	95		95	
		PW package (14 pin)	149			149	
	Operating virtual junction temperature		113	113		113	
T_C	Case temperature for 60 seconds	FK package	150	150	150	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	J or JG package				260	°C
T_{stg}	Storage temperature range		−65 to 150	−65 to 150	−65 to 150	−65 to 150	300 °C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
(6) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

Dissipation Rating Table

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 m/W	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 m/W	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 m/W	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 m/W	546 mW	210 mW

Electrical Characteristics

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A(1)	TL081C TL082C TL084C			TL081AC TL082AC TL084AC			TL081BC TL082BC TL084BC			TL081I TL082I TL084I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	15		3	6		2	3		3	6	mV
			Full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current(2)	V_O = 0	25°C		5	200		5	100		5	100		5	100	pA
			Full range			2			2			2			10	nA
I_{IB}	Input bias current(2)	V_O = 0	25°C		30	400		30	200		30	200		30	200	pA
			Full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			15			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	70	86		75	86		75	86		75	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	70	86		80	86		80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range for TA is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and −40°C to 85°C for TL08_I.

(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

SNOSC25C – MAY 1998 – REVISED MARCH 2013

LM741 Operational Amplifier

Check for Samples: LM741

FEATURES

- Overload Protection on the Input and Output
- No Latch-Up When the Common Mode Range is Exceeded

DESCRIPTION

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance ensured over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Connection Diagrams

LM741H is available per JM38510/10101

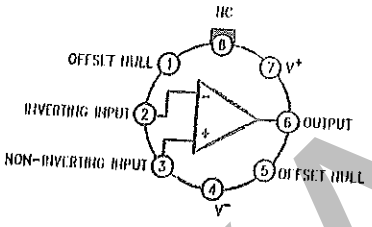


Figure 1. TO-99 Package
See Package Number LMC0008C

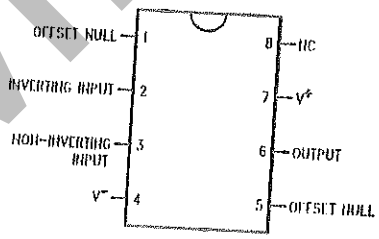


Figure 2. CDIP or PDIP Package
See Package Number NAB0008A, P0008E

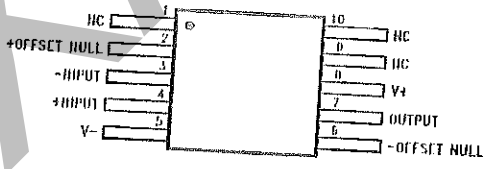


Figure 3. CLGA Package
See Package Number NAD0010A

Typical Application

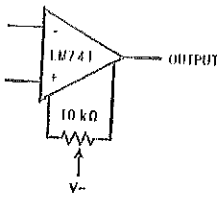


Figure 4. Offset Nulling Circuit

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (4)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (5)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	150°C	100°C
Soldering Information			
P0008E-Package (10 seconds)	260°C	260°C	260°C
NAB0008A- or LMC0008C-Package (10 seconds)	300°C	300°C	300°C
M-Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C
ESD Tolerance (6)	400V	400V	400V

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) For military specifications see RETS741X for LM741 and RETS741AX for LM741A.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.
(5) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
(6) Human body model, 1.5 kΩ in series with 100 pF.

Electrical Characteristics (1)

Parameter	Test Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C										
	$R_S \le 10$ kΩ					1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$		0.8	3.0							
	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 50\Omega$			4.0							mV
	$R_S \le 10$ kΩ						6.0			7.5	
Average Input Offset Voltage Drift				15							µV/°C

(1) Unless otherwise specified, these specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0°C ≤ T_A ≤ +70°C.

Electrical Characteristics[1] (continued)

Parameter	Test Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage Adjustment Range	T_A = 25°C, V_S = ±20V	±10				±15			±15		mV
Input Offset Current	T_A = 25°C		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	T_A = 25°C		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	T_A = 25°C, V_S = ±20V	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, V_S = ±20V	0.5									
Input Voltage Range	T_A = 25°C							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					
Large Signal Voltage Gain	T_A = 25°C, $R_L \ge 2$ kΩ										V/mV
	V_S = ±20V, V_O = ±15V	50									
	V_S = ±15V, V_O = ±10V				50	200		20	200		
	$T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2$ kΩ,										V/mV
	V_S = ±20V, V_O = ±15V	32									
	V_S = ±15V, V_O = ±10V				25			15			
	V_S = ±5V, V_O = ±2V	10									
Output Voltage Swing	V_S = ±20V										V
	$R_L \ge 10$ kΩ	±16									
	$R_L \ge 2$ kΩ	±15									
	V_S = ±15V										V
	$R_L \ge 10$ kΩ				±12	±14		±12	±14		
	$R_L \ge 2$ kΩ				±10	±13		±10	±13		
Output Short Circuit Current	T_A = 25°C	10	25	35		25			25		mA
	$T_{AMIN} \le T_A \le T_{AMAX}$	10		40							
Common-Mode Rejection Ratio	$T_{AMIN} \le T_A \le T_{AMAX}$										dB
	$R_S \le 10$ kΩ, V_{CM} = ±12V				70	90		70	90		
	$R_S \le 50\Omega$, V_{CM} = ±12V	80	95								
Supply Voltage Rejection Ratio	$T_{AMIN} \le T_A \le T_{AMAX}$, V_S = ±20V to V_S = ±5V										dB
	$R_S \le 50\Omega$	86	96								
	$R_S \le 10$ kΩ				77	96		77	96		
Transient Response	T_A = 25°C, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
Bandwidth [2]	T_A = 25°C	0.437	1.5								MHz
Slew Rate	T_A = 25°C, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	T_A = 25°C					1.7	2.8		1.7	2.8	mA
Power Consumption	T_A = 25°C										mW
	V_S = ±20V		80	150							
	V_S = ±15V					50	85		50	85	

(2) Calculated value from: BW (MHz) = 0.35/Rise Time (µs).

FAIRCHILD
SEMICONDUCTOR

www.fairchildsemi.com

LM2903,LM393/LM393A,LM293A

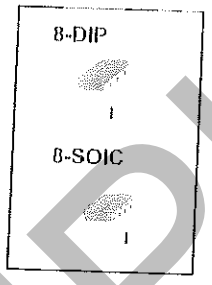
Dual Differential Comparator

Features

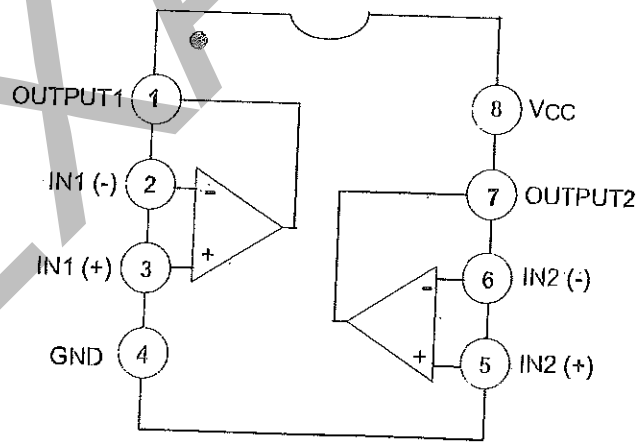
- Single Supply Operation: 2V to 36V
- Dual Supply Operation: ±1V to ±18V
- Allow Comparison of Voltages Near Ground Potential
- Low Current Drain 800μA Typ.
- Compatible with all Forms of Logic
- Low Input Bias Current 25nA Typ.
- Low Input Offset Current ±5nA Typ.
- Low Offset Voltage ±1mV Typ.

Description

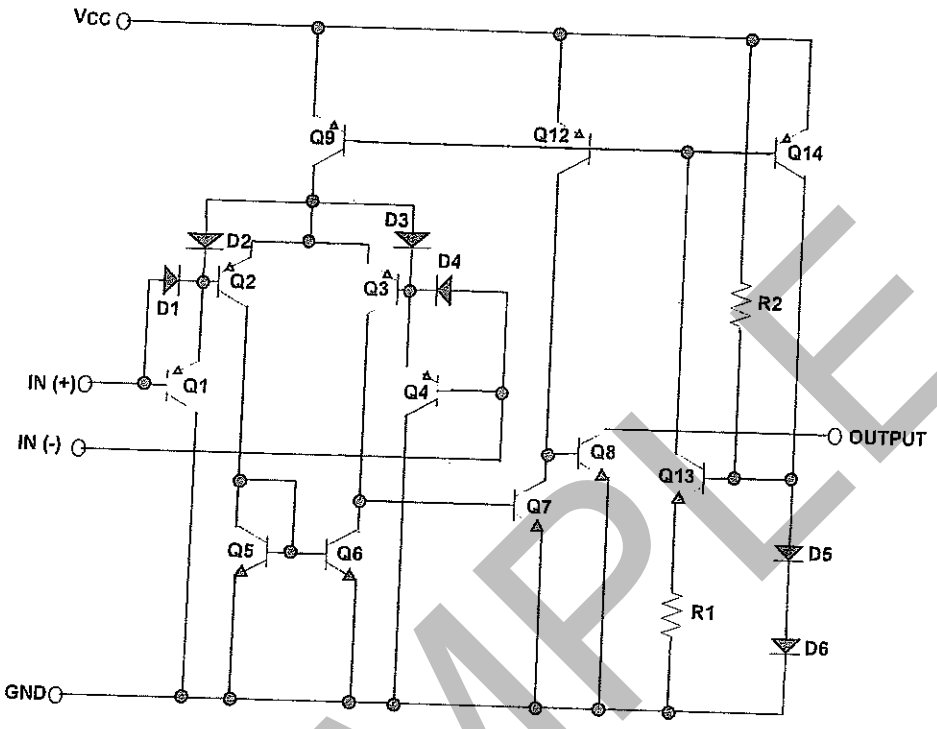
The LM2903, LM393/LM393A, LM293A consist of two independent voltage comparators designed to operate from a single power supply over a wide voltage range.



Internal Block Diagram



Schematic Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	±18 or 36	V
Differential Input Voltage	$V_{I(DIFF)}$	36	V
Input Voltage	V_I	-0.3 to +36	V
Output Short Circuit to GND	-	Continuous	-
Power Dissipation, T_a = 25°C 8-DIP 8-SOIC	P_D	 1040 480	mW
Operating Temperature LM393/LM393A LM2903 LM293A	T_{OPR}	 0 ~ +70 -40 ~ +105 -25 ~ +85	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Ambient Max. 8-DIP 8-SOIC	$R_{\theta ja}$	 120 260	°C/W

Kingbright

T-1 (3mm) SOLID STATE LAMP

Part Number: WP710A10LSECK/J3 Hyper Red

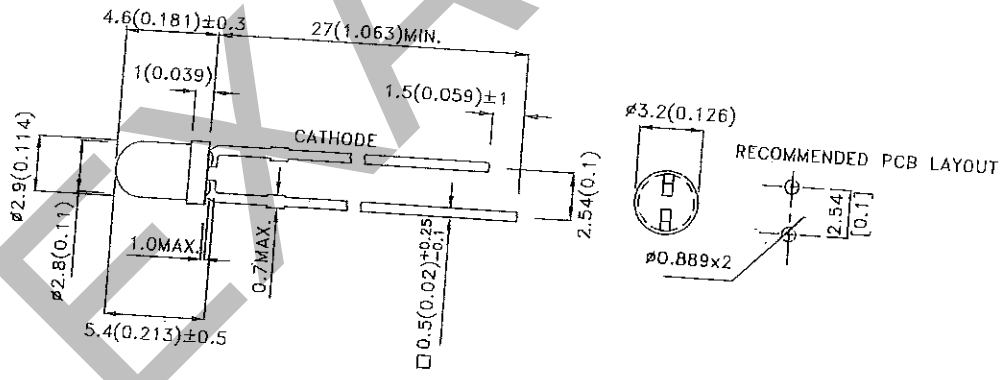
Features

- Low power consumption.
- Popular T-1 diameter package.
- General purpose leads.
- Reliable and rugged.
- Long life - solid state reliability.
- Available on tape and reel.
- Low current IF=2mA operating.
- RoHS compliant.

Description

The Hyper Red device is based on light emitting diode chip made from AlGaInP.

Package Dimensions



Notes:
1. All dimensions are in millimeters (inches).
2. Tolerance is ±0.25(0.01") unless otherwise noted.
3. Lead spacing is measured where the leads emerge from the package.
4. The specifications, characteristics and technical data described in the datasheet are subject to change without prior notice.

Kingbright

Selection Guide

Part No.	Dice	Lens Type	Iv (mcd) [2] @ 2mA		Viewing Angle [1]
			Min.	Typ.	2θ1/2
WP710A10LSECK/J3	Hyper Red (AlGaInP)	Water Clear	180	550	34°
			*120	*320	

Notes:
1. θ1/2 is the angle from optical centerline where the luminous intensity is 1/2 of the optical peak value.
2. Luminous intensity/ luminous Flux: +/-15%.
* Luminous intensity value is traceable to the CIE127-2007 compliant national standards.

Electrical / Optical Characteristics at TA=25°C

Symbol	Parameter	Device	Min.	Typ.	Max.	Units	Test Conditions
λpeak	Peak Wavelength	Hyper Red		640		nm	IF=2mA
λD [1]	Dominant Wavelength	Hyper Red		625		nm	IF=2mA
Δλ1/2	Spectral Line Half-width	Hyper Red		20		nm	IF=2mA
C	Capacitance	Hyper Red		27		pF	VF=0V;f=1MHz
VF [2]	Forward Voltage	Hyper Red	1.5	1.8	2.1	V	IF=2mA
IR	Reverse Current	Hyper Red			10	uA	VR = 5V

Notes:
1.Wavelength: +/-1nm.
2.Forward Voltage: +/-0.1V.
3.Wavelength value is traceable to the CIE127-2007 compliant national standards.
4.Excess driving current and/or operating temperature higher than recommended conditions may result in severe light degradation or premature failure.

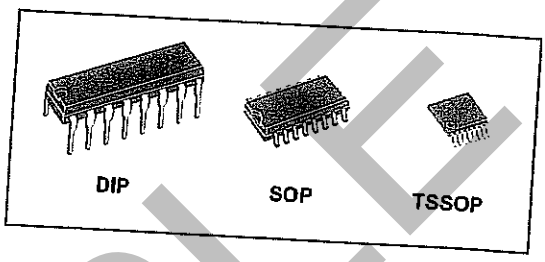
Absolute Maximum Ratings at TA=25°C

Parameter	Hyper Red	Units
Power dissipation	63	mW
DC Forward Current	30	mA
Peak Forward Current [1]	150	mA
Reverse Voltage	5	V
Operating/Storage Temperature	-40°C To +85°C	
Lead Solder Temperature [2]	260°C For 3 Seconds	
Lead Solder Temperature [3]	260°C For 5 Seconds	

Notes:
1. 1/10 Duty Cycle, 0.1ms Pulse Width.
2. 2mm below package base.
3. 5mm below package base.

QUAD D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED :
  t_{PD} = 16 ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} =4μA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 4mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 175



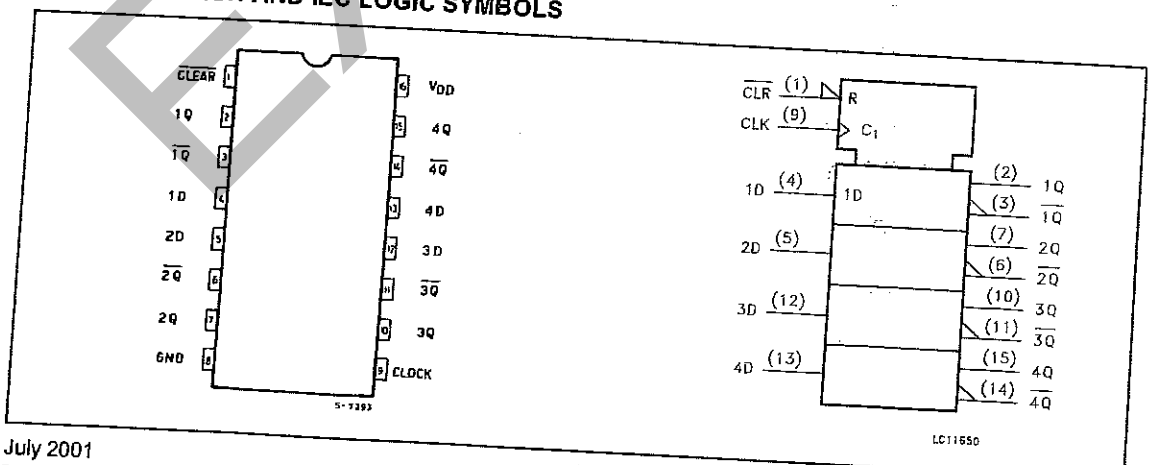
ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC175B1R	
SOP	M74HC175M1R	M74HC175RM13TR
TSSOP		M74HC175TTR

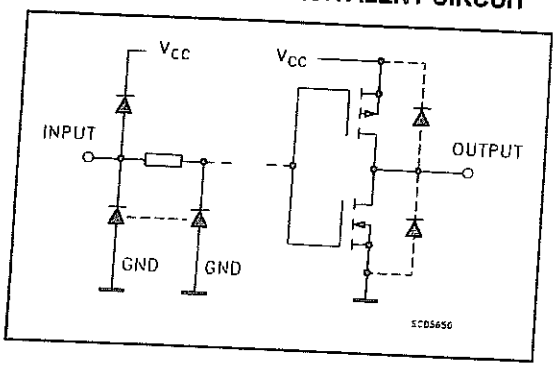
DESCRIPTION

The M74HC175 is an high speed CMOS HEX D-TYPE FLIP FLOP WITH CLEAR fabricated with silicon gate C^2MOS technology.
These four flip-flops are controlled by a clock input (CLOCK) and a clear input ($\overline{CLEAR}$). The information data applied to the D inputs (1D to 4D) are transferred to the outputs (1Q to 4Q and $1\overline{Q}$ to $4\overline{Q}$) on the positive-going edge of the clock pulse. The reset function is accomplished when the $\overline{CLEAR}$ input is low and all Q outputs are low regardless of other input conditions.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

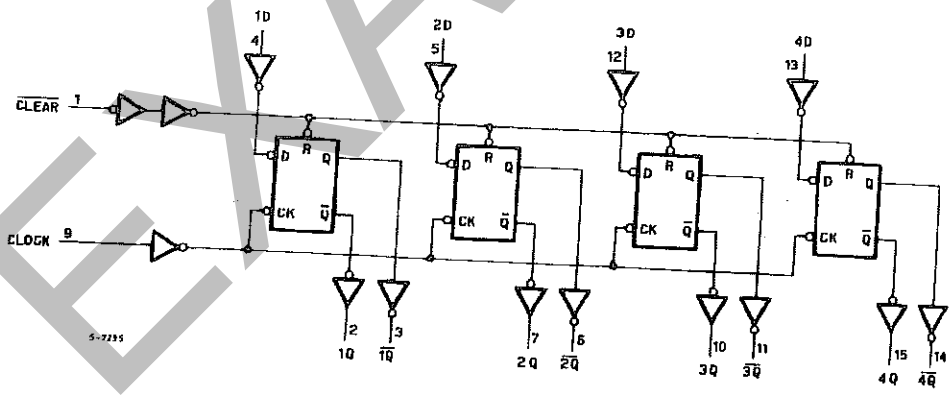
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{CLEAR}$	Asynchronous Master Reset (Active Low)
2, 7, 10, 15	1Q to 4Q	Flip-Flop Outputs
3, 6, 11, 14	$1\overline{Q}$ to $4\overline{Q}$	Complementary Flip-Flop Outputs
4, 5, 12, 13	1D to 4D	Data Inputs
9	CLOCK	Clock Input (LOW to HIGH, edge triggered)
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	$\overline{Q}$	
L	X	X	L	H	
H	L	⌐	L	H	
H	H	⌐	H	L	
H	X	⌙	Qn	$\overline{Qn}$	NO CHANGE

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

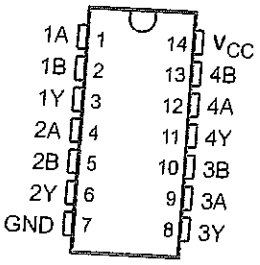
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

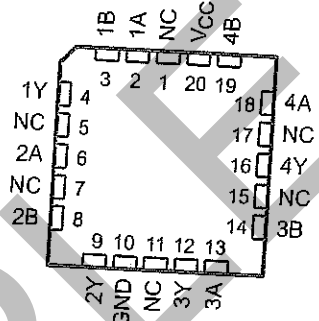
SCLS064E – NOVEMBER 1988 – REVISED AUGUST 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20-μA Max I_{CC}
- Typical t_{pd} = 13 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Inputs Are TTL-Voltage Compatible

SN54HCT32 . . . J OR W PACKAGE
SN74HCT32 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCT32 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HCT32 devices contain four independent 2-input OR gates. They perform the Boolean function $Y = \overline{A} \circ \overline{B}$ or $Y = A + B$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HCT32N	SN74HCT32N
	SOIC – D	Tube of 50	SN74HCT32D	HCT32
		Reel of 2500	SN74HCT32DR	
		Reel of 250	SN74HCT32DT	
	SOP – NS	Reel of 2000	SN74HCT32NSR	HCT32
	SSOP – DB	Reel of 2000	SN74HCT32DBR	HT32
	TSSOP – PW	Tube of 90	SN74HCT32PW	HT32
		Reel of 2000	SN74HCT32PWR	
		Reel of 250	SN74HCT32PWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCT32J	SNJ54HCT32J
	CFP – W	Tube of 150	SNJ54HCT32W	SNJ54HCT32W
	LCCC – FK	Tube of 55	SNJ54HCT32FK	SNJ54HCT32FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HCT32			SN74HCT32			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8			0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time				500			500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SNx4HC14 Hex Schmitt-Trigger Inverters

Check for Samples: SN54HC14, SN74HC14

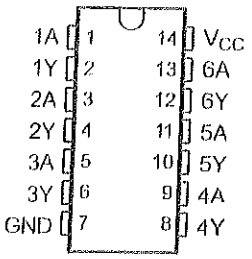
FEATURES

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up to 10 LSTTL Loads
- Low Power Consumption, 20-µA Max I_{CC}
- Typical t_{pd} = 11 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 µA Max

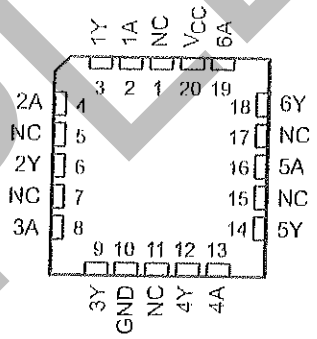
DESCRIPTION

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function Y = A in positive logic.

SN54HC14 . . . J OR W PACKAGE
SN74HC14 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC14 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

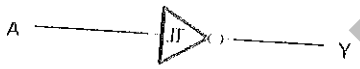
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Function Table (Each Inverter)

INPUTS A	OUTPUT Y
H	L
L	H

Logic Diagram (Positive Logic)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±150	mA
θ_{JA}	Package thermal impedance(3)	D package		86	°C/W
		DB package		96	
		N package		80	
		NS package		76	
		PW package		113	
T_{stg}	Storage temperature range		−60	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

		SN54HC14			SN74HC14			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature	−55		125	−40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC14		SN74HC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+}			2 V	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
			6 V	2.1	3.3	4.2	2.1	4.2	2.1	4.2	
V_{T-}			2 V	0.3	0.6	1	0.3	1	0.3	1	V
			4.5 V	0.9	1.6	2.45	0.9	2.45	0.9	2.45	
			6 V	1.2	2	3.2	1.2	3.2	1.2	3.2	
$V_{T+} - V_{T-}$			2 V	0.2	0.6	1.2	0.2	1.2	0.2	1.2	V
			4.5 V	0.4	0.9	2.1	0.4	2.1	0.4	2.1	
			6 V	0.5	1.3	2.5	0.5	2.5	0.5	2.5	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		6 V			2		40		20	μA
C_I			2 V to 6 V		3	10		10		10	pF

Switching Characteristics

over operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC08		SN74HC08		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		55	125		190		155	ns
			4.5 V		12	25		38		31	
			6 V		11	21		22		26	
t_t			2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

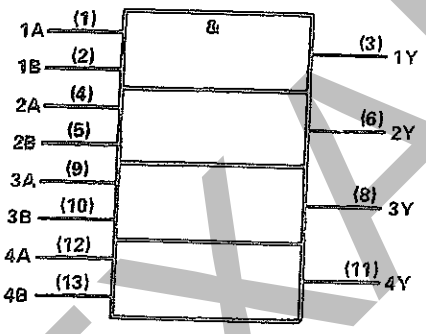
These devices contain four independent 2-input AND gates.

The SN5408, SN54LS08, and SN54S08 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7408, SN74LS08 and SN74S08 are characterized for operation from 0° to 70°C.

FUNCTION TABLE (each gate)

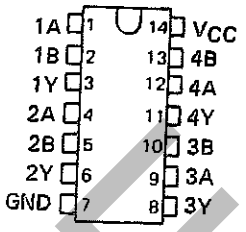
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

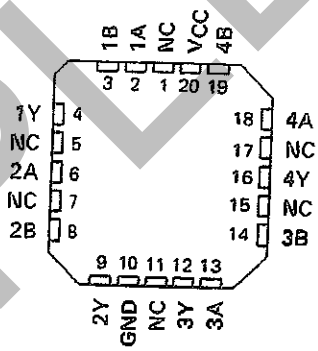


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

SN5408, SN54LS08, SN54S08 . . . J OR W PACKAGE
SN7408 . . . J OR N PACKAGE
SN74LS08, SN74S08 . . . D, J OR N PACKAGE
(TOP VIEW)

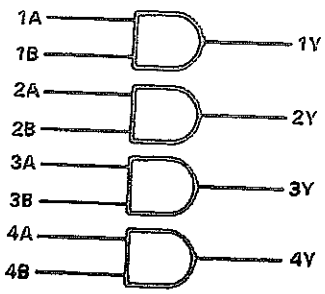


SN54LS08, SN54S08 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

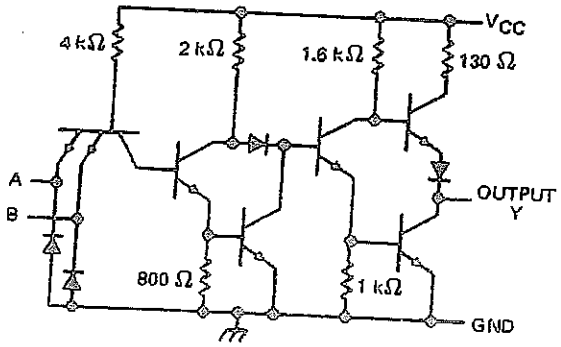
logic diagram (positive logic)



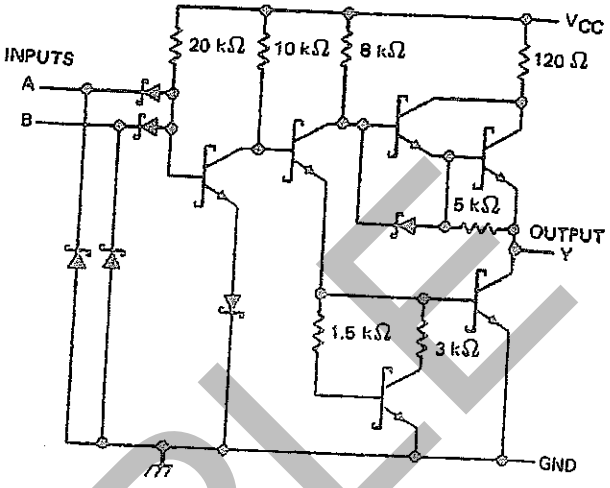
$Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$

schematics (each gate)

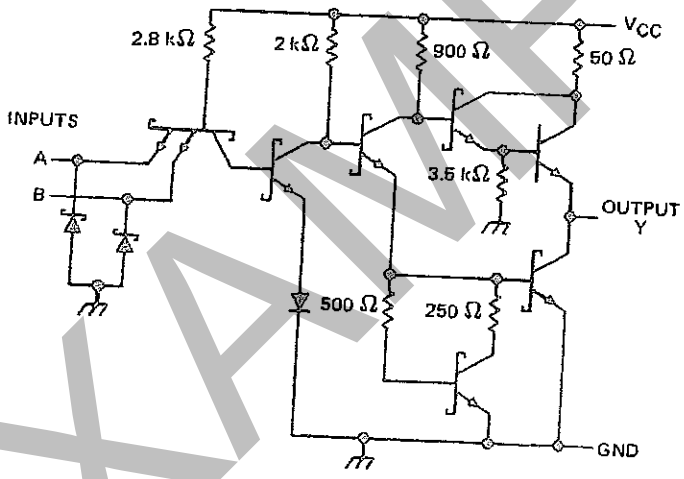
'08



'LS08



'S08



Resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '08, 'S08 . . . . . 7 V
'LS08 . . . . . 5.5 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5408			SN7408			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			– 0.8			– 0.8	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5408			SN7408			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = – 12 mA			– 1.5			– 1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = – 0.8 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			– 1.6			– 1.6	mA
I_{OS}§	V_{CC} = MAX	– 20		– 55	– 18		– 55	mA
I_{CCH}	V_{CC} = MAX, V_I = 4.5 V		11	21		11	21	mA
I_{CCL}	V_{CC} = MAX, V_I = 0 V		20	33		20	33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		17.5	27	ns
t_{PHL}					12	19	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.