2-day National Workshop on

System-On-Chip Architecture for Mixed Mode Applications (SoCAMMA, 2018)

with an Emphasis on Field Programmability for Rapid Prototyping

[23-24 March, 2018]

@ Amrita School of Engineering, Amrita Vishwa Vidyapeetham, Bangalore Campus, Kasavanahalli, Bangalore, 560035

Program Schedule

Day 1 (23 March, Friday), 2018		
Time		
08:30-09:30	Registration	
9:30-10:00	Inauguration	
10:00-10:45	**Dr PV Ananda Mohan** VP (Retd) CDAC	Invited talk –
10:45-11:15	**Tea Break**	
11:15-12:00	**Hitesh Garg,** NXP India	"Ultra Low power Trends in Semiconductor Products and new directions for Analog Building Blocks"
12:00-12:45	**Ms Swathi G** Texas Instrument	SoC Design and Testing
12:45-13:45	**Lunch**	
13:45-16:30	**Ms Vidya Vishwnathan** **Amod Anandkumar,** Mathworks Inc.	Designing and Implementing Advanced Signal Processing Systems using MATLAB and Simulink *with the leverage of HDL Coder™ and HDL Verifier™ to explore design choices to accelerate your FPGA and ASIC verification,*
15:00-15:15	Tea Break	
Day 2 (24 March, Friday), 2018		
9:00-9:45	**Prof Subajit Sen** IIIT Bangalore	Digitally Assisted Analog & Mixed Signal Design
9:45-10:30	**Dr Ganesan Thiagrajan** CTO, MMRFIC	Embedded RF Design
10:30-11:00	**Tea Break**	
11:00-11:45	**Dr Javed GS** Terminus Circuits Pvt Ltd	SerDes Design
11:45-12:40	**Dr. Pratap Kumar Das**, Achronix Semiconductor Corp	Embedded FPGA
12:40-13:45	**Lunch**	
13:45-17:00	**Mr. Rajesh et. al.,** **Oppila Microsystems**	Demo on Anadigm's FPAA (Field Programmable Analog Array)
15:30-16:00	**Tea Break**	