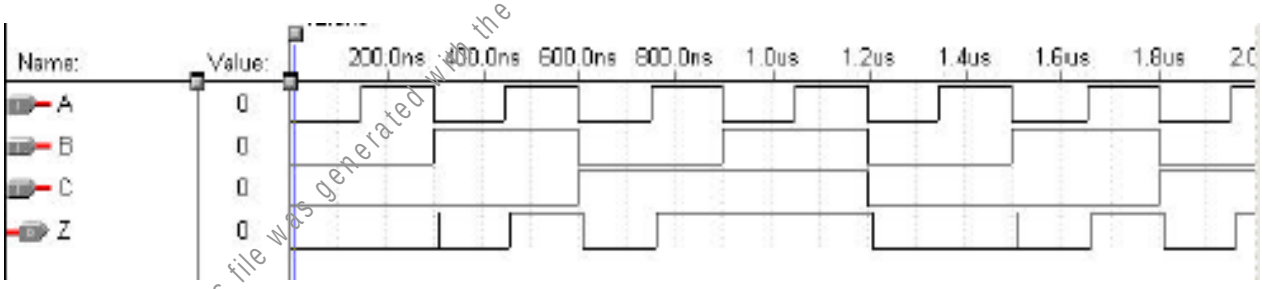
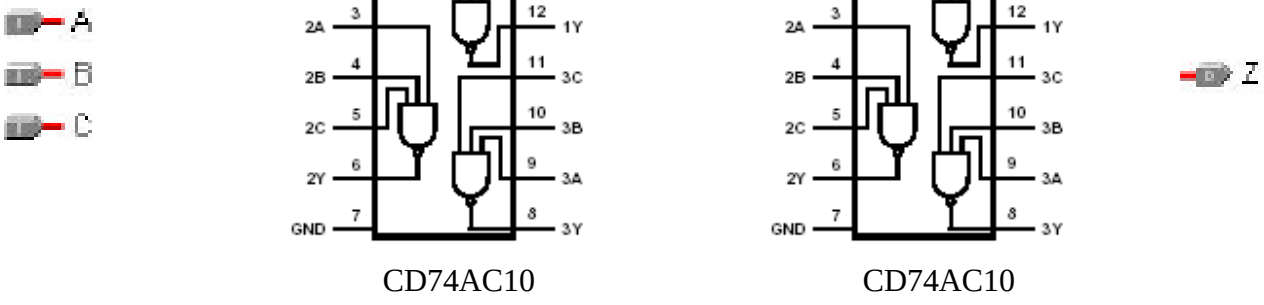
EE292.2 **Final Examination** Date: April 04, 2002

Instructor: **A. Dinh** Student Name: _____
Room: **2C82** Student #: _____
Time: **45 minutes**
*Note: Return this booklet to Room **2C82** upon completing*

Question 1: A technician sets up a circuit with two CD74AD10 (triple 3-input NAND gate) chips and obtains the waveform show below using a logic analyzer. A, B, C are the inputs and Z is the output. Show his connection by drawing the lines connecting the inputs and the output to the two CD74AD10 and the inter-connections between the chips.

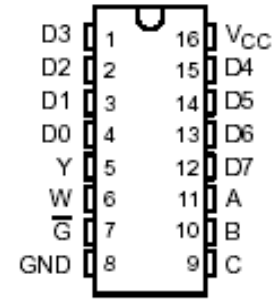




CD74AC10 CD74AC10

Question 2: Show the connection of a **74HC151 MUX** used to implement the following Boolean function

Z(A,B,C) = AB+BC+AC



SN54HC151 . . . FK PACKAGE
(TOP VIEW)

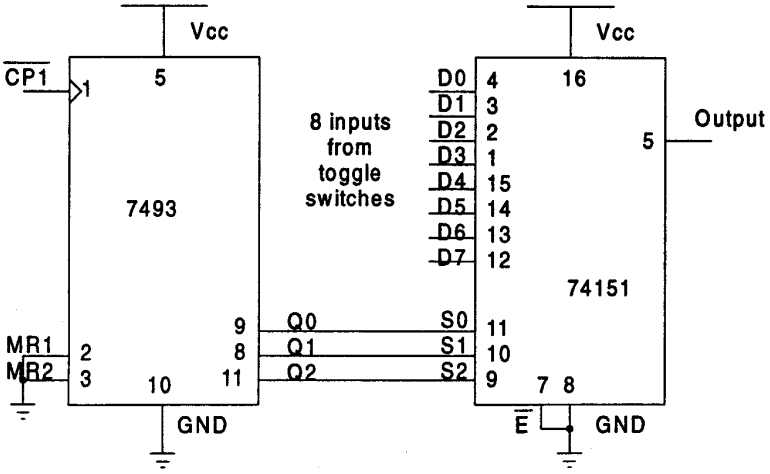
FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE $\overline{G}$	Y	W
C	B	A			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

D0, D1 . . . D7 = the level of the respective D input

Question 3: *(Time allowed 12 minutes)*

For this question, the circuit has been set-up (mark the set-up number in your paper). Pin 1 of the 7493 3-bit counter is connected to a 1kHz, $2.5V_{0\text{-}P}$ square wave. Using the provided logic analyzer or oscilloscope, display the waveforms on pin 5, 9, 10 and 11 of the 74LS151. From the waveforms, determine its input word (D_0 to D_7).



Set-up #: _____

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7

EE292.2	**Final Examination**	Date: April 04, 2002
Instructor: **M. Fotuhi-Firuzabad**		Student Name: _____
Room: **2C70**		Student #: _____
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Q1. Three identical impedances can be connected either as a three-phase delta or as a three-phase wye load. For a given balanced three-phase supply, the power dissipation in the delta configuration will be _____ times that of the power dissipation in the Y configuration.

(a) 3 (b) $\sqrt{3}$ (c) 1/3 (d) $1/\sqrt{3}$

Q2. The power factor angle of a balanced three-phase load is the angle between its:

(a) Line current and the line voltage

(b) Phase current and the corresponding line voltage

(c) Phase current and the corresponding phase voltage.

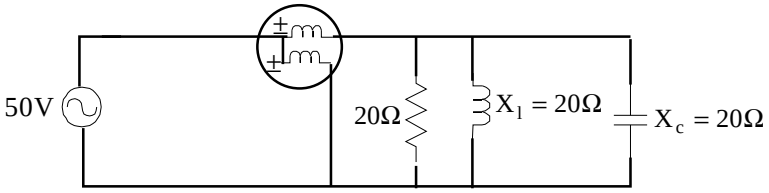
Q3. Mark true (T) or false (F):

(a) The two-wattmeter method cannot be used to measure the total power in an unbalanced 3-phase load.

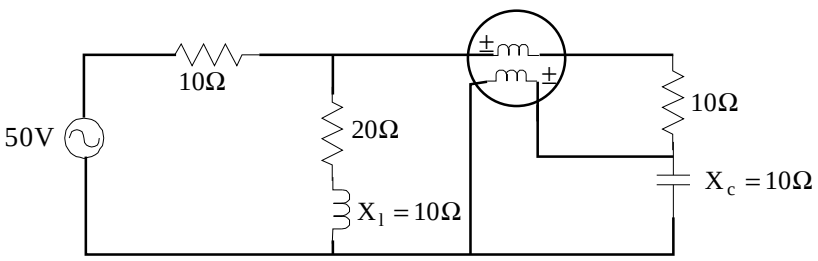
(b) The current in the neutral wire of a balanced Y-to-Y connection is zero.

(c) The algebraic sum of the three phase voltages in a balanced, sinusoidal 3-phase system is zero.

Q4. What should the wattmeters read in the following circuits?



P= _____



P= _____

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Room: **2C70**		Student #: _____
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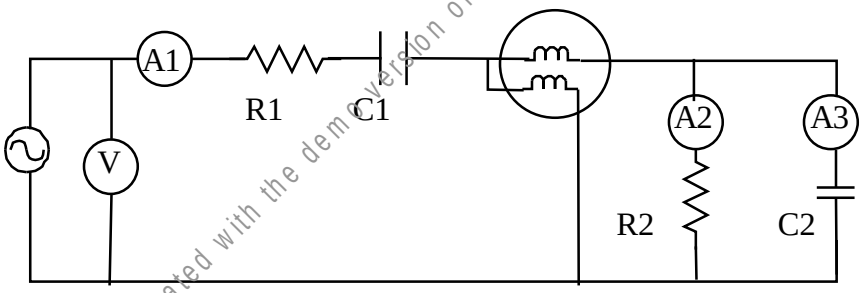
Q5. The circuit shown below has been set-up. In this circuit, R1=32Ω and C1=80μF.



Using readings from the meters, determine:

a. Total active power in Watts.
b. R2 and C2.
c. Total reactive power.
d. Power factor of the circuit.

EE292.2	**Final Examination**	Date: April 04, 2002
Instructor: **A. S. Mehr**		Student Name: _____
Room: **2C72**		Student #: _____
Time: **45 minutes**		
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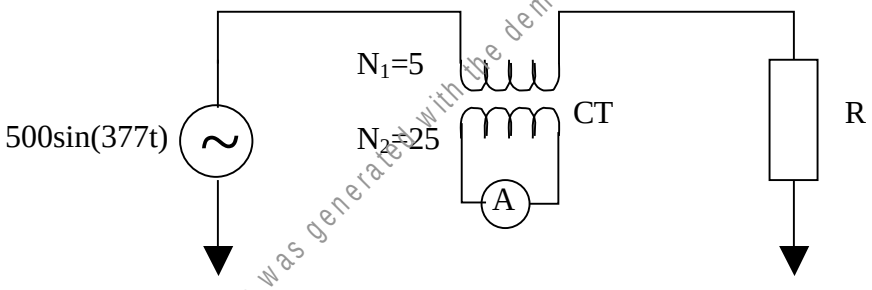
Question 1: (4 points)

In the following figure, the ammeter has the reading of 11.2(A). Find the resistance of the load (R).



Question 2: (14 points)

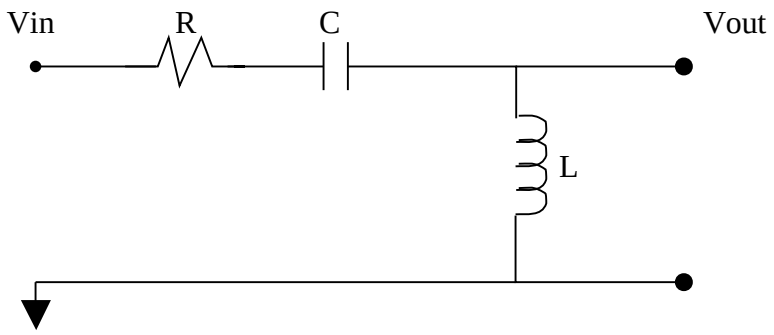
A 1.5KVA, 110V, 60Hz single-phase transformer gave the following test results:

i. Open-circuit test, low potential winding excited
   V_{OC} = 110V, I_{OC}= 0.4A, P_{OC}= 25W, V_{HP} = 220V
ii. Short-circuit test, low potential winding excited
   V_{SC} = 8.25V, I_{SC} = 13.6A, P_{SC}= 40W
iii. Direct-current winding resistances
   R_{LP} = 0.113, R_{HP} = 0.413Ω

a. Determine the equivalent circuit of the transformer referred to the low potential.
b. Determine the full-load efficiency when the transformer is supplying at 110V, a load circuit with a lagging power factor of 0.8.

Question 3: (7 points)

An RLC circuit with the following schematic is provided in the box. Connect this circuit to a (1.1V, 2.0 KHz) power supply. Find the output voltage.

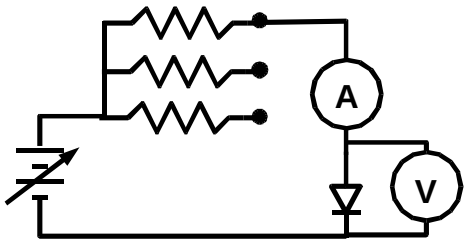


EE292.2 **Final Examination** Date: April 04, 2002

Instructor: **D. Lynch** Student Name: _____
Room: **2C80** Student #: _____
Time: **45 minutes**
*Note: Return this booklet to Room **2C80** upon completion*

1) (*Time allowed: 15 minutes*)

Determine 'n' for the unknown diode connected in the circuit (similar to that shown at right).

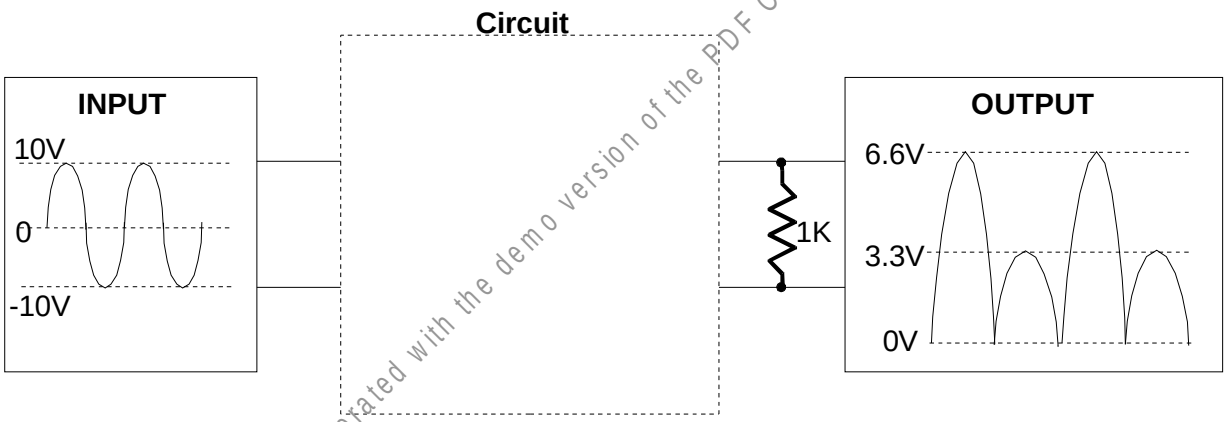


Recall that: $I \approx I_S e^{\frac{qV}{nkT}}$

n = _____

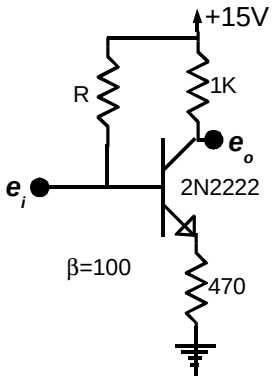
2) (*Time allowed: 15 minutes*)

a) Design and draw the schematic for a diode – resistor circuit that will give an output approximately as shown when connected to a $10V_{0\text{-}P}$ sinusoidal input waveform. (Assume ideal diodes – i.e. a forward biased voltage drop of approximately 0V



b) Determine a value of R in the schematic shown at right that will bias the circuit such that e_o=4.5V_{DC} when the input is not connected.

R = _____



3) (*Time allowed: 15 minutes*)

Use the setup provided (approximately as shown at right) to determine β_{AC} for the transistor in question.

β_{AC} = _____