Midterm up to ?

EF331 Term 1, 2006

QUIZ # 2

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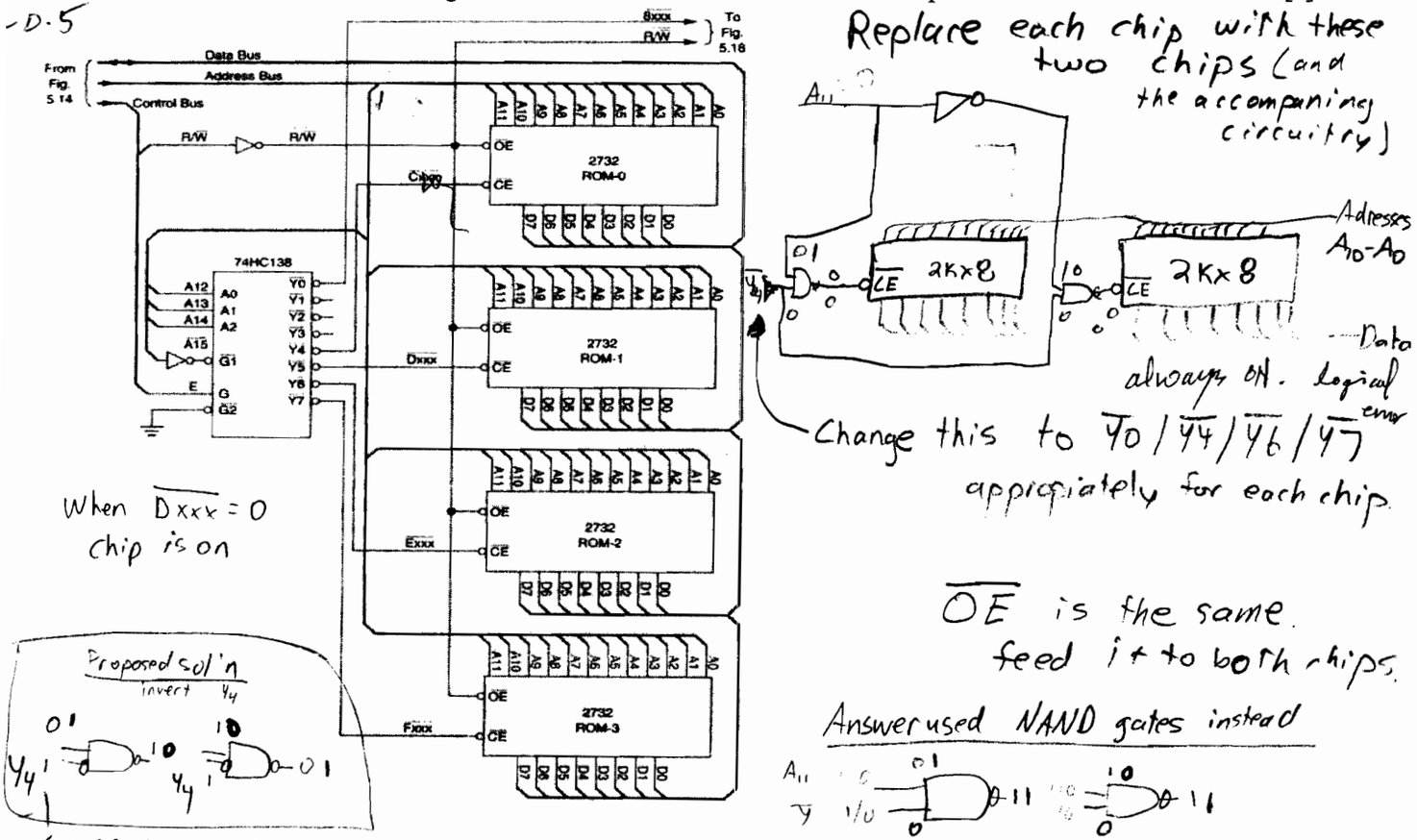
- *45 Minutes, No materials are allowed. [Number] indicates weighting.*

6.25/10

1. 68HC11 has 4 different operating modes. Which one is not one of them? [0.5]
a)single chip mode b)normal expanded mode c)bootstrap mode d)special test mode e)interrupt mode
2. Which port functions as an output port (through A0-A7) and an input/output port (through D0-D7)? [0.5]
~~a)port A~~ b)port B c)port C ~~d)port D~~ ~~e)port E~~
3. Explain why 68HC11 does not increment [PC] on the rising edge of every PH2 clock? [0.5]
- not all clock cyles need PC incremented, such as execute. Only fetch needs PC incremented
4. The circuit of Figure 5.17 uses 2732 EPROMs, each of which is organized as 4K × 8. Modify the circuit so that it uses 2716 EPROMs, each of which is organized as 2K × 8. The total ROM address space is still to be C000 to FFFF. [1]

-0.5



5. Modify the RAM decoding logic of Figure 5.14 as shown in Figure 5.16. Then determine the address ranges for RAM module-2. [1]

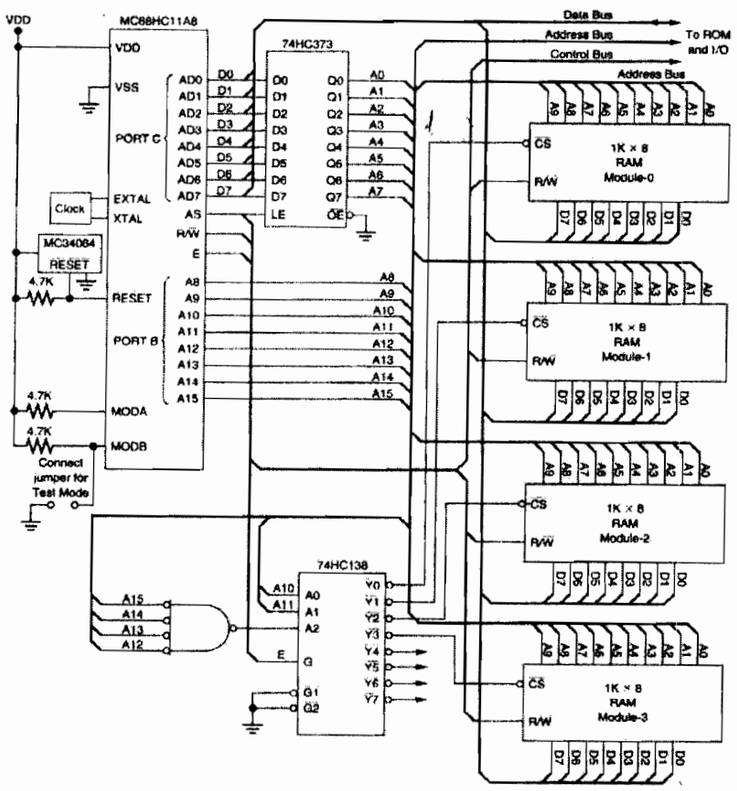


FIGURE 5.14 Typical RAM decoding logic in a 68HC11-based MPU.

{7} = 73A3 to 73A7

002A →

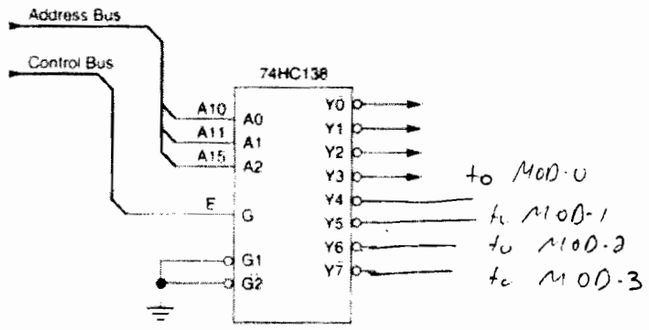


FIGURE 5.16 Modification to Figure 5.14 to achieve partial decoding.

Address Range MOD-2
$\overline{V_6}$ = 1 when $A_{15}A_{11}A_{10}$ 110
i.e. A_{15} = 1
A_{11} = 1
A_{10} = 0

10 xx range = 8-C

1(800) → 1(CFF)

Address Range for MOD-2

1xxx → 8-F

6. How many READ operations does 68HC11 perform when it fetches and executes ~~LDAA~~ $0331? How many write operations? [0.5]

LDAA
address
address
get contents.

READ: 3 Ans: 4
WRITE 0

1xxx 800 – 1xxx CFF

Ans:
8800 – 8CFF
9800 – 9CFF
⋮ ⋮
F800 – FCFF

7. Which one of the following is not related to memory mapped I/O? [0.5]
a) same instructions for I/O and memory b) more programming flexibility
c) easy to program d) full addresses are available

8. Instruction Register? [0.5]
~~a) stores operand addresses~~ b) stores instruction addresses c) stores data addresses d) stores op codes

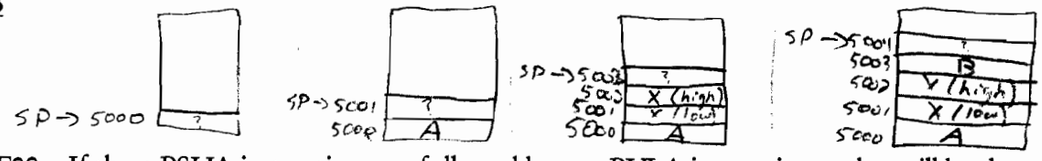
9. During conditional branch instructions, the contents of which register are examined to determine the next sequence of instructions to be performed? [0.5]

CCR Condition code register

10. Consider the following program and assume that the stack pointer register is initially with 5000_{16}. Show the contents of the stack after each instruction. What are the contents of the stack pointer register at the end of the execution of the three push instructions. [2]
PSHA, PSHX, PSHB

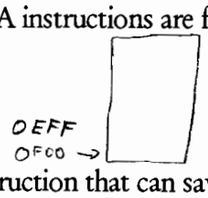
Initial State After PSHA After PSHX After PSHB

SP = 5004
after the 3 pushes



11. Assume that [SP] = $0F00_{16}$. If three PSHA instructions are followed by two PULA instructions, what will be the new [SP]? [1]

0F01

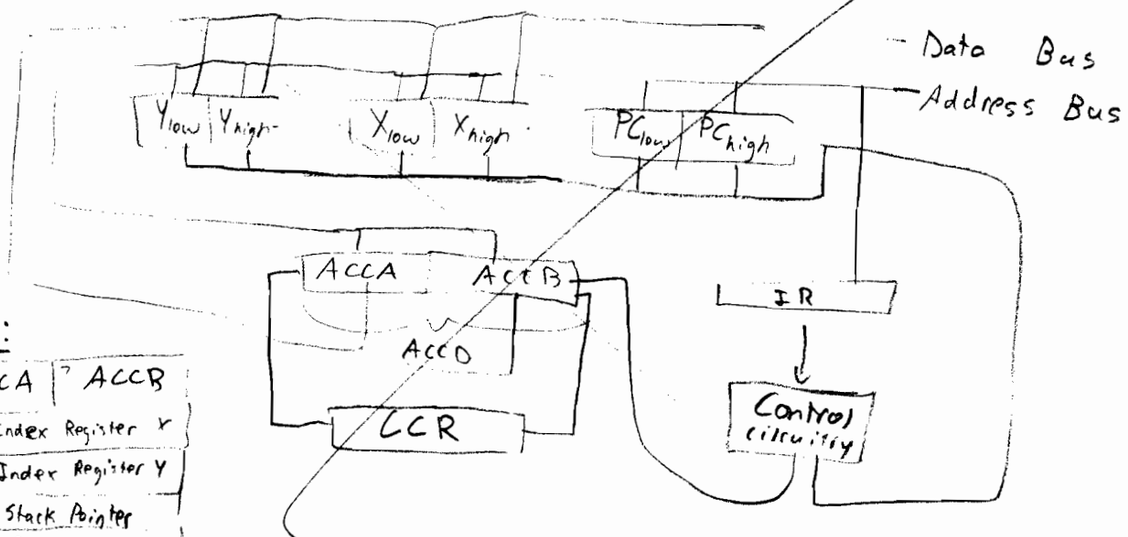


∴ Ans = 0EFF

12. 68HC11 instruction set has no single instruction that can save or push the contents of the condition code register onto the stack. Write a program that will push the contents of the CCR onto the stack. [1]

Store CCR to ACCA (I don't know this exact instruction) Ans: TPA
PSHA

13. Sketch the 68HC11 MPU programming model. [0.5]



Ans:
? ACCA
? ACCB
15 Index Register X
15 Index Register Y
15 Stack Pointer
15 Program Counter
CCR SXHINZVC