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- 45 Minutes. Only calculator is allowed. [Number] indicates weighting
- No interaction with another student is allowed during the exam. Cheating will not be tolerated.

~~9.5~~ / 10
9.5
9.8

1. Which address mode requires no bytes following the op code? [0.5]
Inherent

2. List the five columns that exist in a typical listing of an assembly language program. [0.5]
PC LABEL OP CODE OPERAND COMMENT

-0.2 label address mnemonic comments op code

3. Why are there no instructions for transferring [X] to [ACCA] or [ACCB]? [0.5]
X is 16 bit. Accumulators are 8 bit. X won't fit in ACCA or ACCB

4. There is a group of 5 data bytes stored in memory locations 0270 through 0274. We want to transfer these bytes into memory locations 03A3 through 03A7. Consider two ways (straightforward manner (using LDAAs and STAAs) and indexed addressing (using index registers X and Y)) to implement it. The required number of bytes for all necessary instruction codes is as follows: LDAA (3: extended addressing, 2: indexed (register X) addressing), STAA (3: extended addressing, 2: indexed (register Y) addressing), LDX (3), LDY (4), INX (1), INY (2), CPX (3), BNE (2). Provide the sequence of instruction codes for both ways. Provide the number of required bytes for both ways as well. Use index register X to point to source address. Use index register Y to point to destination address. [3]

1st way: brute force:
LDAA #0270 3
STAA #03A3 3
LDAA #0271 3
STAA #03A4 3
LDAA #0272 3
STAA #03A5 3
LDAA #0273 3
STAA #03A6 3
LDAA #0274 3
STAA #03A7 3
Total Bytes = 30

2nd way: indexed Bytes:
LDX 0270 3
LDY 03A3 4
LDAA \$00, X 2
STAA \$00, Y 3
LDAA \$01, X 2
STAA \$01, Y 3
LDAA \$02, X 2
STAA \$02, Y 3
LDAA \$03, X 2
STAA \$03, Y 3
LDAA \$04, X 2
STAA \$04, Y 3
Total = 35

3rd way: use a loop
LDX 0270 3
LDY 03A3 4
LDAA \$00, X 2
STAA \$00, Y 3
INY 2
INX 1
CPX #0275; 3
BNE LABEL 2
WAS 2
Total # of bytes = 20

5. Fill out the following table to calculate the exact delay for the delay subroutine. Answer the total cycles and delay, too. Assume that [X] is set to 1. [4]

Instruction	Cycles/Execution	# Executions	Total Cycles
start LDY #011C	4	1	4
loop DEY	4	\$011C = 284	1136
BNE loop	3	\$011C = 284	852-1 = 851
DEX X=1 → X=0	3	1	3
BNE start	2(no branch)	1	2
RTS	5	1	5

(b/c BNE only needs 2 bytes when it doesn't branch, which happens once.)

$\Sigma = 2001$

TOTAL CYCLES: 2001, DELAY: 1.0005ms = 10 005 μs

6. Provide two lines of instruction code for clearing TOF. TOF is the most significant bit in address \$1025. [0.5]

LDAA #80 ; 1000 0000
STAA \$1025

7. When is the timer overflow flag set? [0.5]

When TCNT goes from FFFF to 0000.

8. How long does it take for the TCNT to count from \$0000 to \$FFFF? Explain the reason, too. Assume that the E-clock is 2 MHz and prescale factor is 1. [0.5]

$$= \left(\frac{1}{2 \text{ MHz}} \right) \cdot (65,535) (1) = 32.77 \text{ ms}$$

$$(2^{16} - 1)$$

Survey: Which one do you prefer?

1. Any point (probably somewhere in ch. 9) that we will reach to with a normal pace.
2. Finish chapter 9 with a fast pace.

