EE431 Quiz No. 3: Written

Date: Thursday, November 29, 2001
Time = 40 minutes
Texts and Notes allowed

1. Generate a schematic diagram for the Verilog descriptions given below. For the flip/flops in your schematic, use a D type with clock enable, asynchronous set and asynchronous clear.

(1) (a)
```
module circuit_1 (clk, a, b, c, Q)
input clk, a, b, c;
output Q;
reg Q;
always @ (posedge clk)
begin
if (a == 1'b1) Q <= 1'b1
else if (b == 1'b1) Q <= c;
else Q <= c ^ Q;
end
```

(1) (b)
```
module circuit_2 (clk, a, b, c, d, r)
input clk, a, b, r;
input [1:0] c;
output  d;
reg Q1, Q2, d;
always @ (posedge clk or negedge r)
if (r == 1'b0)  begin Q1 <= 1'b0; Q2 <= 1'b0; end
else
if ( a == b)
   case (c)
   2'b00: begin Q1 <= c[1];    Q2 <= Q1; end
   2'b01: begin Q1 <= d ^ Q2; Q2 <= b;  end
   2'b10: begin Q1 <= d;      Q2 <= Q1; end
   2'b11: begin Q1 <= d;      Q2 <= Q1; end
   endcase
else begin Q1 <= 1'b0; Q2 <=1'b1; end
```

```
always @ (Q1 or Q2 or d)
if (a == Q2) d = Q1;
else if (Q1 == Q2) d = Q2;
else d = b;

endmodule
```

2. Consider the structural description below

```
module circuit_3(clk, y)
input clk;
output y
wire x, d;
DFFE flop_1 (.clk(clk), .d(d), .Q(x));
DFFE flop_2 (.clk(clk), .d(x), .Q(y));
nor nor_1(d,x,y);
endmodule

DESCRIPTION OF CONNECTION LIST FOR D FLOP
DFFE instance_name (
   .D(d),         // the d input
   .CLK(clk),     // the clock, positive edge trigger
   .ENA(enable), // if used, D goes to Q on clock edge when
                  // ENA is high  otherwise Q does not change
   .CLRN(clear_bar), // if used, clears Q when low
   .PRN(set_bar),    // if used, sets Q when low
   .Q(q)     // output
   );
```

(1) (a) Write a behavioral description in Verilog of the circuit described above. For this description use only blocking equalities in the "always" constructs.

(1) (b) Write a behavioral description in Verilog of the circuit described above. For this description use only non-blocking equalities in the "always" constructs.

3. Consider the structural description below

```
module circuit_4(clk_1, clk_2, y)
input clk_1, clk_2;
output y
wire x, w;
DFFE flop_1 (.CLK(clk_1), .D(1'b1), .CLRN(y), .Q(x));
DFFE flop_2 (.CLK(clk_2), .D(1'b1), .CLRN(y), .Q(w));
nand nand_1 (y,w,x);
endmodule
```

(1) (a) Write a behavioral description in Verilog of the circuit described above. For this description use only blocking equalities in the "always" constructs.

(1) (b) Write a behavioral description in Verilog of the circuit described above. For this description use only non-blocking equalities in the "always" constructs.