

## EE431 First Lab Midterm for 2005

Date: Tuesday, February 8, 2005

Time = 30 minutes

Text Books, Notes and Computer Files Only

1. Write a Verilog description of the circuit described by the block diagram on the page attached. Compile your description for a Flex10k series FPGA. There is no need to select a specific device.

After compiling, open the waveform editor, import the inputs and outputs and then do the following:

- (a) Make the simulation time 1100  $\mu\text{s}$ .
- (b) Make the clock, which is "clk", a square clock with period 1  $\mu\text{s}$ . The clock should start low and make a transition to high at 0.5  $\mu\text{s}$ .
- (c) Make "clear" a pulse that is high for the first  $2.2 \pm 0.1 \mu\text{s}$  and low for the remainder of the simulation.
- (d) Make "seed", the constant 12'H1E9 for the entire time of the simulation.
- (e) Observe the output that occurs while "count" is 12'H3E4. If your circuit is working properly the output should be 12'HD88.
- (f) Change "seed" and report the result as instructed on the answer sheet. The answer sheet will be handed out after you are in the lab.

