EE431 First Lab Midterm for 2005

Date: Tuesday, February 8, 2005
Time = 30 minutes
Text Books, Notes and Computer Files Only

1. Write a Verilog description of the circuit described by the block diagram on the page attached. Compile you description for a Flex10k series FPGA. There is no need to select a specific device.

   After compiling, open the waveform editor, import the inputs and outputs and then do the following:

   (a) Make the simulation time 1100 μs.

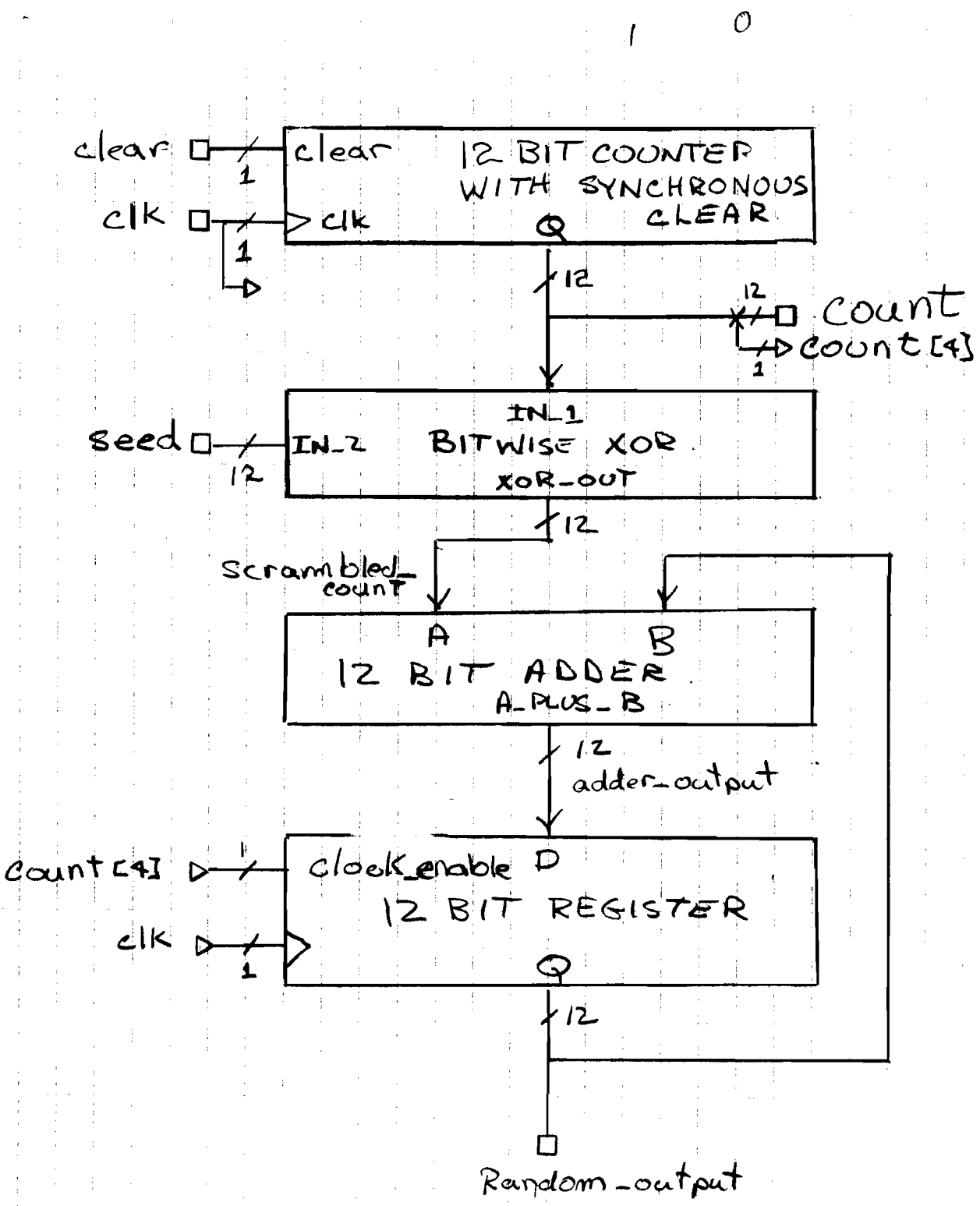
   (b) Make the clock, which is "clk", a square clock with period 1 μs. The clock should start low and make a transition to high at 0.5 μs.

   (c) Make "clear" a pulse that is high for the first 2.2 ± 0.1 μs and low for the remainder of the simulation.

   (d) Make "seed", the constant 12'H1E9 for the entire time of the simulation.

   (e) Observe the output that occurs while "count" is 12'H3E4. If your circuit is working properly the output should be 12'HD88. HD88

   (f) Change "seed" and report the result as instructed on the answer sheet. The answer sheet will be handed out after you are in the lab.


clear
clk
1
1
clear
clk
12 BIT COUNTER
WITH SYNCHRONOUS
CLEAR
Q
12
12
count
count[4]
1
IN_1
seed
IN_2
BITWISE XOR
XOR_OUT
12
12
scrambled_
count
A
B
12 BIT ADDER
A_PLUS_B
12
adder_output
count[4]
1
clock_enable
D
12 BIT REGISTER
clk
1
Q
12
Random_output

ANSWER SHEET

(20) Make the seed 12'H 333 for the entire time of the simulation. Observe "random_output" when "count" is 12'H3E4 and record the value below:

random_output = 12'H ?

0

handed in on time ___

handed in late ✓ overlabt

ANSWER SHEET

NAME:_____

STU.NO.:_____

(20) Make the seed 12'H__111____ for the entire time of the simulation. Observe "random_output" when "count" is 12'H3E4 and record the value below:

random_output = 12'H__44A_____

20