E.E. 451.3/ENEL 489

VLSI/Integrated Circuit Design

1998 Mid-Term Solutions

QUESTION #1

MARKS: 15 (3 + 3 + 3 + 3 + 3)

a) THE POLYSILICON LAYER IS USUALLY USED AS A SIGNAL ROUTING LAYER. GIVE 3 REASONS FOR THIS

- Has relatively low resistance.
- Has relatively low capacitance.
- Is not metal (prevents metal limited designs).
- Signals must be on polysilicon to activate a transistor. Can save a contact cut by keeping signal on polysilicon.

b)

i) None. (IF ANY) EXPLAIN THE DIFFERENCE BETWEEN THE TERMS FIELD, FOX + THICKOXIDE

ii) None. Realizing t_{ox} is actually the thickness. (" + DEVICE WELL, t_{ox} + THINOXIDE)

iii) See previous answers. Field is related to thick-oxide and device well is related to thin-oxide. Diffusion is another name for device well. (" FIELD, DEVICE WELL + DIFFUSION)

See page 118 (etc) in 2nd Edition, page 68 (etc) in 1st Edition, and pages C2, C6 and Figure C.1(e) in Appendix C handout.

c) WHERE IS CANADIAN MICROELECTRONICS CORPORATION (CMC) LOCATED? GIVE 2 COMPANIES (PRIVATE COMPANY TECHNOLOGY) THAT USE FABRICATION FOR CMC.

CMC, Room 210A, Carruthers Hall, Queen's University, Kingston, Ontario, K7L 3N6

Nortel	BiCMOS, CMOS5, FT25 (CMOS3DLM is no longer used)
Mitel	Mitel15
Gennum	GA911
MOSIS	CMOSIS5
Vitesse	GaAs

"So, I want you to get up now. I want all of you to get up out of your chairs. I want you to get up right now and go to the window, open it, and stick your head out and yell, 'I'm mad as hell and I'm not going to take this anymore!'"

N-Channel transistors are characterized as not passing 1's well + p-channel transistors are characterized as not passing 0's well. Explain why.

i)

For n-channel transistors, when Vgs < Vt (typical Vt is on the order of 0.7V), the transistor is in cut-off mode (i.e., off). Given the maximum gate voltage would be Vdd and one side of the transistor connected to Vdd, the largest voltage which could be "passed" would be (Vdd – Vt) (e.g., 4.3V).

Similarly for p-channel transistors, the typical Vt is on the order of –0.7V. Given the minimum gate voltage would be Vss and one side of the transistor connected to Vss, the smallest voltage which could be passed would be (Vss – Vt) (e.g., +0.7V).

See pages 86-87 in text for similar explanation.

e) LIST 3 MODES OF OPERATION OF A MOS TRANSISTOR + BRIEFLY DESCRIBE EACH ONE.

- Cut-off. When Vgs < Vt, the transistor is effectively turned "off" (there is still a small
- Linear. When Vgs >= Vt and Vds < (Vgs – Vt), the current flow is approximately proportional to Vds.
- Saturation. When Vgs >= Vt and Vds > (Vgs – Vt), the current flow is approximately a constant independent of Vds.

Question confused some as should have asked for three "regions" as opposed to modes. Many mixed regions with modes (inversion, accumulation, etc.). So marks were given for either/or.

f) WHY DOES METAL1-FIELD HAS A CAPACITIVE EDGE COMPONENT BUT NOT METAL1 – POLYSILICON OR METAL1 – DIFFUSION?

The field (substate in this case) can be thought of as a large plane relative to the metal1 lines. Therefore you get fringing effects from the perimeter of metal1 to the field "plane". Polysilicon and diffusion are usually relatively small areas on the die and therefore do not act like planes relative to metal1 and thus the fringing effects can usually be ignored.

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QUESTION #2

MARKS: 15 (5 + 5 + 5)

a) Consider the pseudo-Nmos inverter shown below. Given V_{in} = 5V & the max. target V_{out} = 0.2V, what is minimum value of resistor R? It is made of polysilicon, what is the physical size of resister R? Is this a realistic size to implement on an IC?

Given Vout = Vds = 0.2V

Vin = Vgs = 5V

Vt = 0.7V (for an n-channel CMOS3DLM)

Therefore, since Vgs > Vt and Vds < (Vgs – Vt), the transistor is in "linear" mode.

The current flow through a transistor in linear mode is given by:

$$Ids = \beta[(Vgs - Vt)Vds - Vds^2/2]$$

$$\beta = \mu\frac{\varepsilon_{ox}}{t_{ox}}\left(\frac{W}{L}\right)$$

Since the same current that is flowing through the transistor is flowing through the resistor:

$$V_{dd} = I_{ds} \times R + 0.2V$$

$$R = \frac{4.8V}{(755cm^2/V\,sec)\frac{3.9\times8.854\times10^{-14}F/cm}{5\times10^{-6}cm}[4.3\times0.2 - 0.2^2/2]}$$

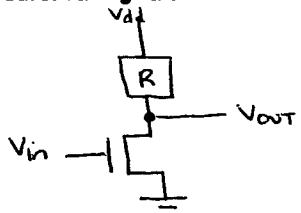
$$R = 106.8k\Omega$$

For polysilicon, resistance = $18\Omega/square$

$$\text{Length in squares} = \frac{106.8k\Omega}{18\Omega/square} = 5933$$

Since minimum poly width = 3um, length = 17,800um (17.8mm)

The length is longer than most chips so this is **NOT** realistic! Could be done as a serpentine but still a **large** area.



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b) Consider a Minimum Sized inverter (MSI) to be the smallest inverter possible w/ equal rise & fall times.

i) What are the sizes of the n-channel & p-channel transistors in such an MSI?

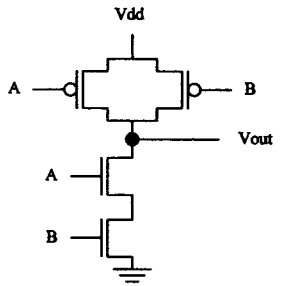
i) For CMOS3DLM, $\mu_n = 775cm^2/Vs$

$\mu_p = 250cm^2/Vs$

Therefore, n-channel: 3um wide by 3um long

p-channel: $\frac{775}{250}\times3 = 9.3$um wide by 3um long

ii) Consider the diagram for a NAND gate:



For Vout = 1, one p-channel transistor will be "pull up" (worst case scenario). Thus the p-channel should be the same size as for the MSI.

For Vout = 0, two n-channel transistors are in series. Thus they must each have half the resistance of the n-channel in the MSI, therefore they must be twice as wide.

n-channel: 6um wide by 3um long

p-channel: 9.3um wide by 3um long

iii) Consider the gate capacitance seen on the input of the two types of gates. The gate capacitance is proportional to the gate area:

For MSI, gate area = 3 x 3 + 9.3 x 3 = 36.9 um^2

For NAND, gate area = 6 x 3 + 9.3 x 3 = 45.9 um^2

Thus the relative speed of driving a NAND versus driving an MSI = 36.9 / 45.9 = 80%

ii) What are the required sizing of the transistor in a 2-input NAND gate which drives an MSI so that it has the same worst case delays as an MSI driving an MSI?

iii) How much slower will the above 2-input NAND gate be driving an identical 2-input NAND gate compared to driving an MSI?

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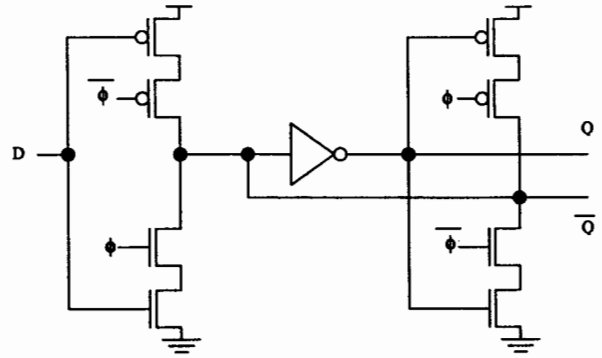
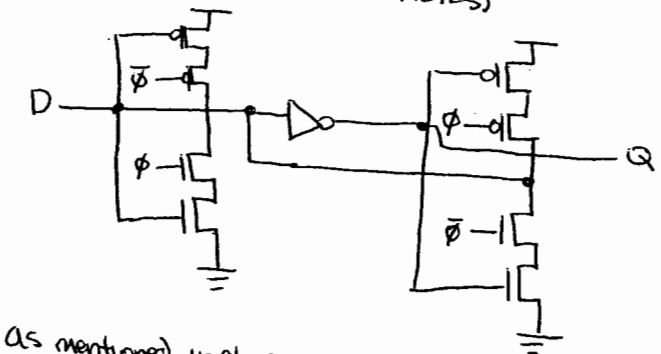
c)

No, the circuit does not function as intended. D is driving against –Q, Q follows –D, and the output from the "first stage" (indicated by "X") does not go anywhere!

The correct circuit should be:



Consider the diagram below: design domain abstraction of a D-type Static Latch. THE circuit is shown (& previously in class notes)



as mentioned in class, sometimes the design domain abstraction loses track of what the designer intended (reality). Does the circuit function as intended? If not, Clearly show your connected circuit.

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QUESTION #3

MARKS: 15 (10 + 5)

Some things to consider:

- Circuit is not correct. I am assuming you are using the correct circuit.
- A STICKS diagram is done using lines, NOT polygons, rectangles, etc. Do NOT show physical layout since this would take way too long.
- Inputs on metal must get to polysilicon. Therefore 3 contact cuts.
- With outputs on metal may need as many as 4 contact cuts.
- Phi and PhiBar need at least 2 contact cuts to swap sides (top to bottom). Maybe as many as 4.
- Each transistor pair (i.e., in an inverter) contains 5 contact cuts. This assumes output is on polysilicon.
- Each transistor set (2 n-channel and 2 p-channel, i.e., in a clocked inverter) contains 5 (NOT 9) contact cuts. This assumes output is on polysilicon.
- With two substate contact of each type there is about 24-30 contact cuts. We may be able to do it with less (if things work out) but it is unlikely.
- A single transistor is about 25 dsm high and about 15 dsm wide. The width can be reduced by "hiding" the polysilicon overlap of diffusion but will still be 9 dsm wide (due to contact cut on source and drain). Rules A.2, A.3, A.6, A.7, C.5, D.7, and Rules A.2, A.6, C.5, and E.1.
- A series combination of two transistors is about 35 dsm high and about 15 dsm wide. The width can be reduced by "hiding" the polysilicon overlap of diffusion but will still be 9 dsm wide (due to contact cut on source and drain). Rules (see above) and B.3.
- V_{DD} and V_{SS} lines are 9dsm wide (due to the contact cuts in them). Rules A.6, C.5.
- Don't forget that p+ diffusion and P-well must be spaced 14 dsm apart. Rule D.1.
- There are two choices for STICKS diagram organization. Vertical transistors and Horizontal transistors. A STICK solution is shown for each. Note that I have left the "white-space" in these diagrams to make them easier to read. It I was to do a physical layout I would concentrate on these spots in order to optimize the size.
- Note that the ϕ and $\overline{\phi}$ signal go from bottom to top and vice versa. If the cells had to be stacked end-to-end, this would allowed the cascading to be done efficiently by automatically making the right connections.

Q draw Sticks diagram for D-type Static Latch from 2 (c).
Correct Circuit if needed.
1. inputs must come in from If. (Met.1)
2. outputs must exit from rt (Met1)
3. Analysis both clock phases (ϕ & $\overline{\phi}$) are generated externally
4. No interconnection wires are allowed outside V_{DD} & V_{SS} power rails.
V_{dd} power rail should be at the top & V_{SS} at the bottom.
5. At least 2 substrate connections (of each type) shown
6. Show p-well
7. No Met.2 allowed
8. Standard Sticks colors for CMOS 3DLM to be used.
- good CMOS circuit design guidelines are to be used.

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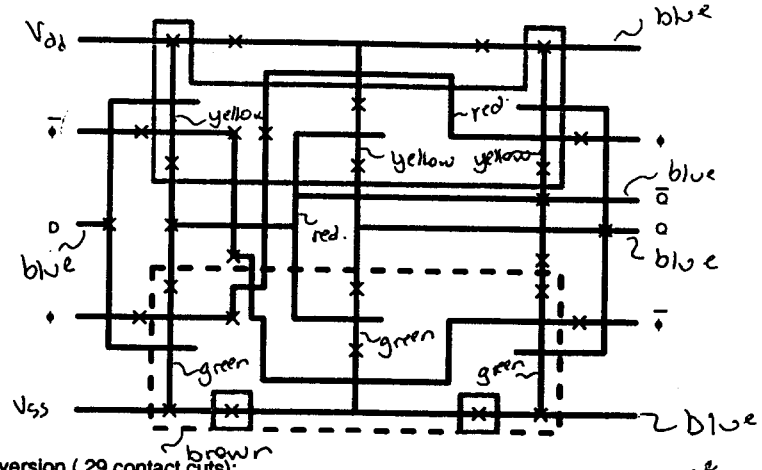
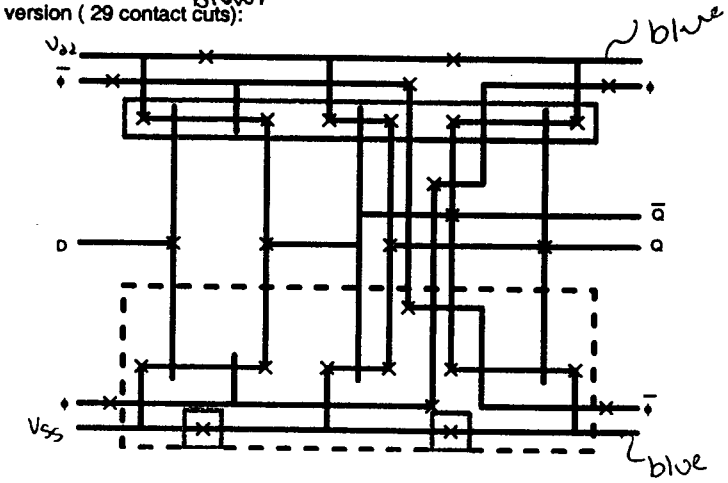
a)

Vertical transistor version (29 contact cuts):



Horizontal version (29 contact cuts):



b)

Horizontal transistors: 9 + 5 + 9 + 14 + 9 + 5 + 9 = 60 dsm

Vertical transistors (worst case): 9 + 35 + 14 + 35 + 9 = 102 dsm

Note that some assumptions have been made about "hiding" some of the connections.

Estimate height, in design scale Microns, of a physical layout based on D-type Sticks diagram. Height is defined as the distance from top Vdd to bottom Vss. Do not do a detailed calculation.

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[Prof] "Any questions?"

[Students] "I don't understand enough of this to formulate