

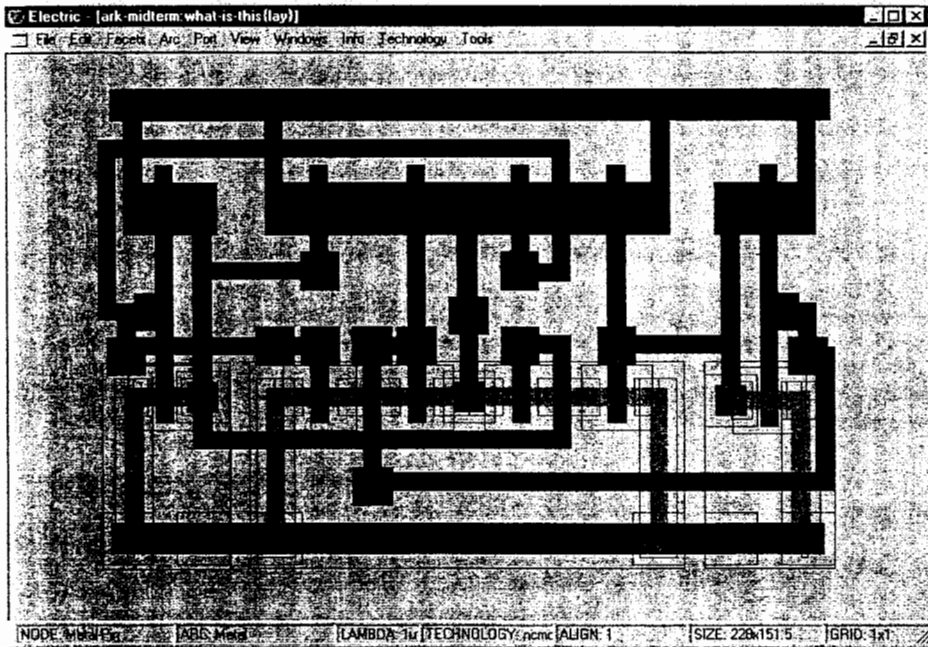
QUESTION #1

MARKS: 15 (5 + 5 + 3 + 2)

Being able to "reverse engineer" the layout of a facet (cell) is an important skill to verify the functionality of the cell as well as to uncover any layout errors. All the parts of this question relate to the diagram of the facet (cell) on this page.

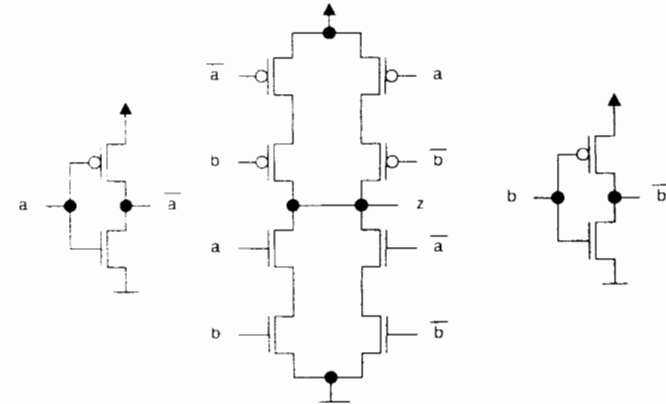
- a) Identify the various layers by running coloured lines through the centre of each polygon (do not bother shading in the whole polygon as that will take too much of your time). Use red for polysilicon, blue for metal1, black for metal2, green for n+ diffusion, yellow/orange for p+ diffusion, brown for p-well, "x" for contact cuts, and "o" for vias. If you need to use additional or different colours, make sure to provide a legend on your diagram

Question #1 a) Work Sheet



Question #1 b), c), d) Work Sheet

1b)



1c)

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

This cell provides an "XOR" function.

1d)

- Two things missing
- Substrate connections to Vdd
  - Connection to GND for middle p-well.

Student Name \_\_\_\_\_

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## QUESTION #2

MARKS: 15 (5 + 5 + 5)

Consider the following three (3) parts of this question. For each of the parts, provide a short explanation. Do all three (3).

- a) Describe two common techniques whereby the oxide of silicon, SiO<sub>2</sub>, is grown on crystalline silicon wafers.

## Question #2 a) Work Sheet

- Wet oxidation. Heating silicon wafers in an oxidizing atmosphere containing water vapour. Temperature usually between 900C and 1000C. This is a rapid process.
- Dry oxidation. The oxidizing atmosphere is pure oxygen. Temperature around 1200C to achieve an acceptable growth rate.

So I jump ship in Hong Kong and make my way over to Tibet, and I get on as a looper at a course over in the Himalayas. A looper, you know, a caddy, a looper, a jock. So, I tell them I'm a pro jock, and who do you think they give me? The Dalai Lama, himself. Twelfth son of the Lama. The flowing robes, the grace, bald... striking. So, I'm on the first tee with him. I give him the driver. He hauls off and whacks one---big hitter, the Lama---long, into a ten thousand foot crevasse, right at the base of this glacier. Do you know what the Lama says? Gunga galunga... gunga, gunga-galunga. So we finish the eighteenth and he's gonna stiff me. And I say, "Hey, Lama, hey, how about a little something, you know, for the effort, you know." And he says, "Oh, uh, there won't be any money, but when you die, on your deathbed, you will receive total consciousness." So I got that goin' for me, which is nice.

Student Name: \_\_\_\_\_

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- b) Describe the behavior of an n-channel transistor in the various regions (i.e., cut-off, linear or triode, and saturation). Include the appropriate I<sub>DS</sub> equations and operating conditions for each region.

## Question #2 b) Work Sheet

- Cut-off. Occurs when V<sub>gs</sub> ≤ V<sub>t</sub>. I<sub>ds</sub> = 0. Transistor is effectively "off".
- Linear. Occurs when 0 < V<sub>ds</sub> < (V<sub>gs</sub> - V<sub>t</sub>).

$$I_{DS} = \beta \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

I<sub>ds</sub> varies roughly linearly with V<sub>ds</sub> for a particular V<sub>gs</sub> (assuming V<sub>ds</sub> << (V<sub>gs</sub> - V<sub>t</sub>)),

Transistor acts almost like a resistor.

- Saturation. Occurs when 0 < (V<sub>gs</sub> - V<sub>t</sub>) < V<sub>ds</sub>.

$$I_{DS} = \beta \left[ \frac{(V_{GS} - V_T)^2}{2} \right]$$

I<sub>ds</sub> is a constant depending on V<sub>gs</sub>. Transistor acts like a constant current source.

Student Name: \_\_\_\_\_

Student Number: \_\_\_\_\_

c) For an n-channel transistor, plot the drain-source current as a function of the drain-source voltage for various selections of the gate-source voltage. Where necessary, use device parameters as indicated on Page 2 of the examination paper.

Question #2 c) Work Sheet

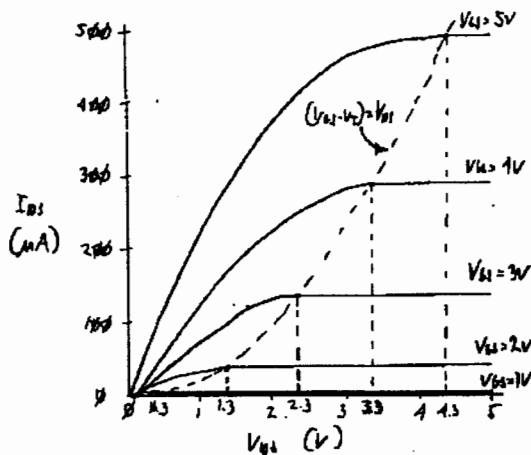
At saturation,

$$I_{DS} = \beta \left[ \frac{(V_{GS} - V_T)^2}{2} \right]$$

$$\beta = \frac{\mu_n C_{ox} W}{L} = \frac{775 \times 3.9 \times 8.85 \times 10^{-14} \times 3 \mu m}{5 \times 10^{-6} \times 3 \mu m} = 5.35 \times 10^{-5}$$

Vgs	Ids (Saturation) (uA)
1	2.4
2	45
3	142
4	291
5	495

Knee between saturation and linear occurs at  $(V_{GS} - V_T) = V_{DS}$



Student Name: \_\_\_\_\_

Student Number: \_\_\_\_\_

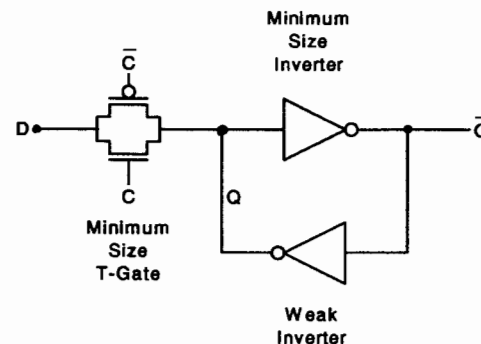
QUESTION #3

MARKS: 15 (7 + 8)

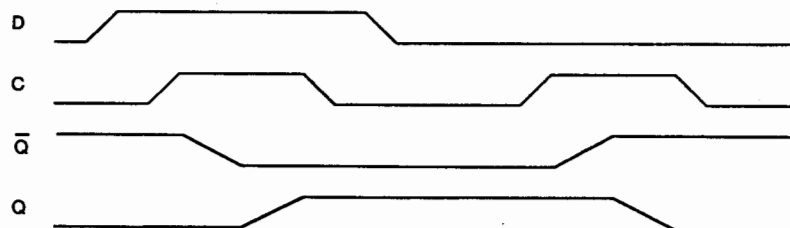
Consider the following circuit. It is a variation of the T-Latch that you analyzed as part of one of your assignments. Note that the T-Gate in the feedback loop is missing and that the inverter in the feedback loop is NOT a Minimum Size Inverter. Instead it has been replaced with a Weak Inverter (also known as a Trickle Inverter).

Note that a CMOS3DLM Minimum Size Inverter has a n-channel pull-down transistor of size  $3\mu m:3\mu m$  (W:L) and a p-channel pull-up transistor of size  $9\mu m:3\mu m$  (W:L). As well a CMOS3DLM Minimum Size T-Gate has a n-channel transistor of size  $3\mu m:3\mu m$  (W:L) in parallel with a p-channel transistor of size  $9\mu m:3\mu m$  (W:L).

In order for this circuit to work properly, the bottom inverter must be a Weak Inverter. A Weak Inverter is one with a low  $\beta$ . The  $\beta$  must be chosen so that the circuit driving the D input can "override" the output of the Weak Inverter if the two output signals (the output of the circuit driving the D input and the output of the Weak Inverter driving the Q node) are in the opposite state. This would occur if the T-Latch was loading a D input that was a complementary value of the Q node (i.e.,  $D=0$  when  $Q=1$  or  $D=1$  when  $Q=0$ ).



See the waveforms below for an illustrative (not to scale) example of the operation of the circuit.



Student Name: \_\_\_\_\_

Student Number: \_\_\_\_\_

a) Assuming the device driving the D input is a Minimum Size Inverter, calculate the  $\beta$  of the Weak Inverter needed for the circuit to operate correctly. Hint: When the T-Latch is changing state, the circuit can effectively be modelled as a resistive voltage divider.

Question #3 a) Work Sheet

IF Q IS LOW:

CIRCUIT LOOKS LIKE TO MAKE HI



Now  $R_{WMSI} = 4.275K$   
 $R_{PMSI} = \frac{13600}{3} = 4.533K$

$$V_A = V_{DD} \left( \frac{R_{WMSI}}{R_{PMSI} + R_{T0} + R_{WMSI}} \right)$$

$$= V_{DD} \left( \frac{N \times R_{WMSI}}{R_{PMSI} + R_{T0} + N \times R_{WMSI}} \right)$$

OR

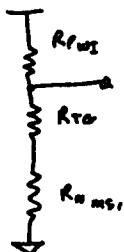
$$N = \frac{V_A}{(V_{DD} - V_A)} \left( \frac{R_{PMSI} + R_{T0}}{R_{WMSI}} \right)$$

$V_A$	$N$
2.5	1.67
3.0	2.36
4.0	6.30
4.2	8.26
4.5	14.20

Use  $N \approx 8$

IF Q IS HI:

CIRCUIT LOOKS LIKE TO MAKE I



$R_{T0} = 4.275K \parallel \frac{13600}{3}$   
 $= 2.2K$   
 $R_{WMSI} = N \times R_{WMSI}$   
 $R_{PMSI} = N \times R_{PMSI}$

$$V_A = V_{DD} \left( \frac{R_{WMSI} + R_{T0}}{R_{PMSI} + R_{T0} + R_{WMSI}} \right)$$

$$= V_{DD} \left( \frac{R_{WMSI} + R_{T0}}{R_{PMSI} + R_{T0} + N \times R_{WMSI}} \right)$$

OR

$$N = \frac{(V_{DD} - V_A)}{V_A} \left( \frac{R_{WMSI} + R_{T0}}{R_{PMSI}} \right)$$

$V_A$	$N$
2.5	1.42
2.0	2.14
1.0	5.7
0.7	8.75
0.5	12.85

Use  $N \approx 8$

Student Name: \_\_\_\_\_

Student Number: \_\_\_\_\_

b) As well as determining the  $\beta$  of the Weak Inverter, the clock signal, C, must satisfy certain criteria. In particular the length of time the C input is asserted (i.e., logical 1) must be long enough for the output and Q node to stabilize. Calculate the minimum length of time the C input must be asserted for the circuit of Part 3 a) to work properly.

Assume the following (you may also make other appropriate assumptions):

- Assume 0ns propagation delay from the C input to the input/output of the T-Gate.
- Assume 2ns rise and fall times of the C input.
- Assume the D input has stabilized before the C input is asserted.
- Assume that the only load capacitances are the gate capacitances of the transistors.
- Assume 10%-90% (90%-10%) rise (fall) times are the same as the 0%-100% (100%-0%) rise (fall) times.

Question #3 b) Work Sheet

$$t_{r \approx} \frac{4}{\beta} C_L \rightarrow \text{ACTUALLY } \frac{3.3466 C_L}{\beta V_{DD}}$$

$$t_{f \approx} \frac{1}{\beta} C_L \rightarrow \text{ACTUALLY } \frac{3.455 C_L}{\beta V_{DD}}$$

$10C_g = 6.2 \times 10^{-15} f$   
 $= 3 \times 3 \times 6.9 \times 10^{-4} pf/\mu m^2$

$M_1 \text{ LOAD} = 4 \times 10C_g = 24.8 ff$

$\beta p = 3 \times 17.2 \times 10^{-6} A/V^2 = 51.6 \times 10^{-6} A/V^2$

$M_2 \text{ LOAD} = 8 \times M_1 \text{ LOAD} = 198.4 ff$

$\beta n = 53.5 \times 10^{-6} A/V^2$

ASSUME NO RESISTIVE EFFECT THROUGH TGATE.

ASSUME Q IS LOW

ASSUME Q IS HI

$$t_D = \frac{2\tau_0}{2} + \frac{t_{rA}}{2} + \frac{t_{fB}}{2} + \frac{2\tau_0}{2}$$

$$= 1ns + \frac{.7 \times 24.8ff}{2 \times 51.6 \times 10^{-6}} + \frac{.8 \times 198.4ff}{2 \times 53.5 \times 10^{-6}} + 1ns$$

$$= (1 + .192 + .840 + 1) ns$$

$$= 3.67 ns$$

$$t_D = \frac{2\tau_0}{2} + \frac{t_{rA}}{2} + \frac{t_{fB}}{2} + \frac{2\tau_0}{2}$$

$$= 1ns + \frac{.8 \times 24.8ff}{2 \times 51.6 \times 10^{-6}} + \frac{.8 \times 198.4ff}{2 \times 53.5 \times 10^{-6}} + 1ns$$

$$= (1 + .155 + 1.54 + 1) ns$$

$$= 3.72 ns$$

I AM ASSUMING THAT I DON'T HAVE TO WAIT WHILE THE WEAK INVERTER COMPLETES ITS TRANSITION SINCE Q NODE IS ALREADY DRIVEN TO CORRECT STATE.

I AM ALSO ASSUMING THAT THE C INPUT CAN BE REMOVED 1NS LATER.

Student Name: \_\_\_\_\_

Student Number: \_\_\_\_\_

“WHAT ARE YOU LOOKING AT?  
 HAVEN'T YOU EVER SEEN A  
 MAN SO BROKEN THAT HE JUST  
 HAD TO SPIN?”