EE 451 / ENEL 489
Assignment # 1
Due: Thursday February 10, 2000

Question # 1: Integrated Circuit Fabrication

a) What are the two common means of oxidization?

b) Consider an n-type silicon substrate, the doping concentration being $10^{15}cm^{-3}$. This substrate is then ion implanted with a dose of $10^{12}cm^{-2}$ Boron atoms to a depth of 1μm. Assuming that the ions which result from this implantation are uniformly distributed over the area and depth of the implant, what is the polarity of the resultant material and what is its effective dopant concentration?

c) Why does the use of polysilicon lead to a "self-aligning" of the source and drain regions?

Question # 2 : Ideal Current-Voltage Characteristics

a) Plot the ideal current-voltage characteristics of an n-MOS silicon transistor. Assume that μ_n=775cm^2/Vs, $\varepsilon_s=3.9\varepsilon_o$, $t_{ox}=5\times10^{-8}$m, W=3μm, and L=3μm; ε_o denotes the dielectric constant associated with vacuum. Assume a threshold voltage of 1V.

b) Plot the ideal current-voltage characteristics of a p-MOS silicon transistor. Assume that μ_n=250cm^2/Vs, $\varepsilon_s=3.9\varepsilon_o$, $t_{ox}=5\times10^{-8}$m, W=3μm, and L=3μm; ε_o denotes the dielectric constant associated with vacuum. Assume a threshold voltage of 1V.

Question # 3 : Nonidealities

a) Plot the current-voltage characteristics, corresponding to the transistors discussed in Question # 2, except now take into account channel modulation. Assume that $\lambda=0.01V^{-1}$ for the case of the n-channel device and that $\lambda=0.03V^{-1}$ for the case of the p-channel device.

b) Plot the drift velocity of electrons in silicon, v_d, as a function of the applied electric field, F, if

$$v_d = \frac{\mu_n \times F}{\sqrt{1+(\frac{\mu_n \times F}{v_s})^2}}$$

where μ_n denotes the low field mobility, 775cm^2/Vs, and v_s denotes the saturation drift velocity, 10^7cm/s.

Question 1a: Two common means of oxidation (growing SiO_2):

* Wet oxidation: Oxidizing atmosphere contains water vapor. Temperature between 900°C and 1000°C. Rapid process.
* Dry oxidation: Oxidizing atmosphere contains pure oxygen. Temperature around 1200°C. Acceptable growth rate.

Question 1b:

$$\text{Doping concentration of Boron} = \frac{10^{12}cm^{-2}}{1\mu m} = \frac{10^{12}cm^{-2}}{10^{-4}cm} = 10^{16}cm^{-3}$$

Boron donates p type, so as the doping concentration of the boron is higher than the n-type substrate, the resulting material will be p-type.

Effective doping concentration $=10^{16}cm^{-3} - 10^{15}cm^{-3} = 9\times10^{15}cm^{-3}$ (p-type)

Question 1c:

The use of polysilicon is referred to as "self-aligned" as since the polysilicon is placed prior to the substrate doping, the polysilicon defines the gates of the transistors. The drains and sources cannot extend underneath the polysilicon.

Question 2a:

Need to use design equations:

$$I_{ds} = 0 \qquad , V_{gs} < V_t$$

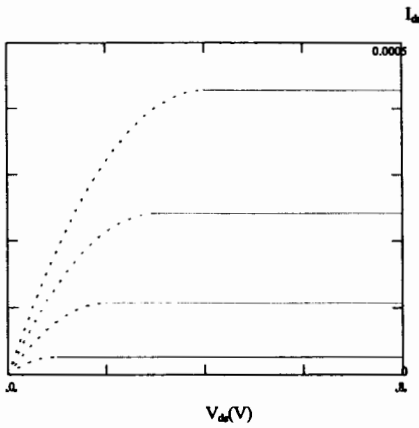
$$I_{ds} = \beta\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \qquad , V_{ds} < (V_{gs} - V_t)$$

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2 \qquad , V_{ds} > (V_{gs} - V_t)$$

$$\beta = \mu\frac{\varepsilon_{ox}}{t_{ox}}\left(\frac{W}{L}\right) = 775\frac{cm^2}{Vs}\times\frac{3.9\times8.85\times10^{-14}\frac{F}{cm}}{500\times10^{-8}cm}\times\left(\frac{3\mu m}{3\mu m}\right) = 53.5\frac{\mu A}{V^2}$$

Below is the plot of the ideal current-voltage characteristics of the n-MOS transistor. The plot shows 4 levels of Vgs (2,3,4 and 5 Volts). The dot lines indicate $V_{ds} < (V_{gs}-V_t)$ and the solid lines indicate $V_{ds} > (V_{gs}-V_t)$.

"I don't ask you to understand fractions. All we ask is for you to press a few buttons on your calculator. You don't even need to like fractions. See if I care."

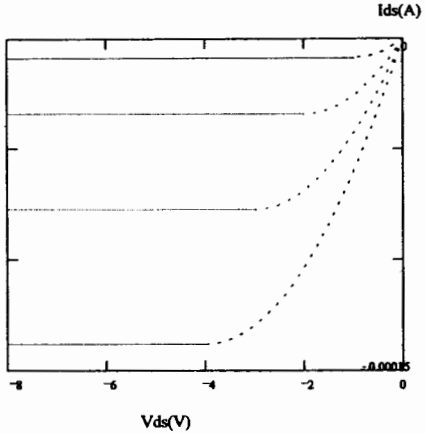


Question 2b:

The new β has to be calculated for p-MOS as:

$$\beta = -\mu \frac{\varepsilon_{ox}}{t_{ox}}\left(\frac{W}{L}\right) = 250\frac{cm^2}{Vs} x \frac{3.9x8.85x10^{-14}\frac{F}{cm}}{500x10^{-8}cm} x\left(\frac{3\mu m}{3\mu m}\right) = -17.26\frac{\mu A}{V^2}$$

Below is the plot of the ideal current-voltage characteristics of the p-MOS transistor. The plot shows 4 levels of Vgs (-2,-3,-4 and -5 Volts). The dot lines indicate $V_{ds} < (V_{gs}-V_t)$ and the solid lines indicate $V_{ds} > (V_{gs}-V_t)$.



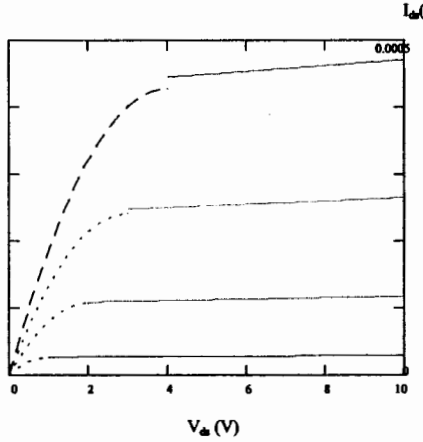
Question 3a:

A new equation for I_{ds} is used if the channel modulation is taken into account:

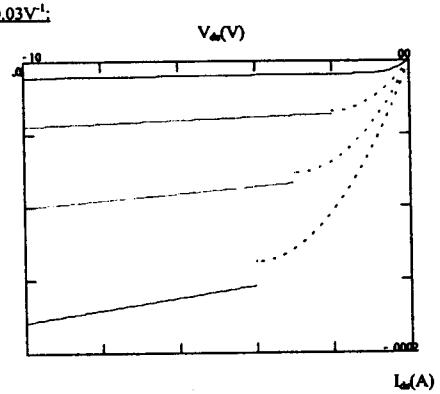
$$I_{ds} = [\frac{\beta}{2}(V_{gs} - V_t)^2](1 + \lambda V_{ds})$$

On the plots, the solid lines show the effect of channel modulation on the saturated currents. (compared with question2a and 2b plots).

n-MOS λ=0.01V^{-1}:



p-MOS λ=0.03V^{-1}:

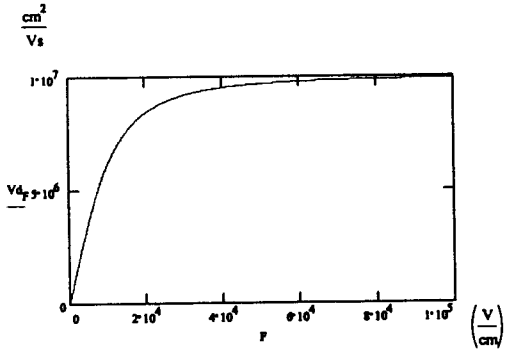


Question 3b:

Use the equation for drift velocity of electrons in silicon, v_d:

$$v_d = \frac{\mu_n \cdot F}{\sqrt{1+\left(\frac{\mu_n \cdot F}{v_s}\right)^2}}$$

The plot of the drift velocity (V_d) versus applied electric field (F) is shown below:



EE 451 / ENEL 489
Assignment # 2
Due: Thursday February 17, 2000

1. (2 marks) Create a "STICKS" diagram of a 2-input CMOS NAND gate with the following parameters:
   a) Input ports "in1" and "in2" accessible on metal2.
   b) Output port "out" accessible on metal2.
   c) Power port "vdd" on metal1.
   d) Ground port "gnd" on metal1.
   e) Include at least one substrate and one P-well connection.

   Use "standard" CMOS3DLM colours and symbols for layers:

Layer	Colour / Symbol
Metal1	Blue
Metal2	Black
Polysilicon	Red
N+ Diffusion	Green
P+ Diffusion	Yellow/Orange
P-well	Brown
Contact Cut	Black "X"
Via	Black "O"

   Hand in your STICKS diagram.

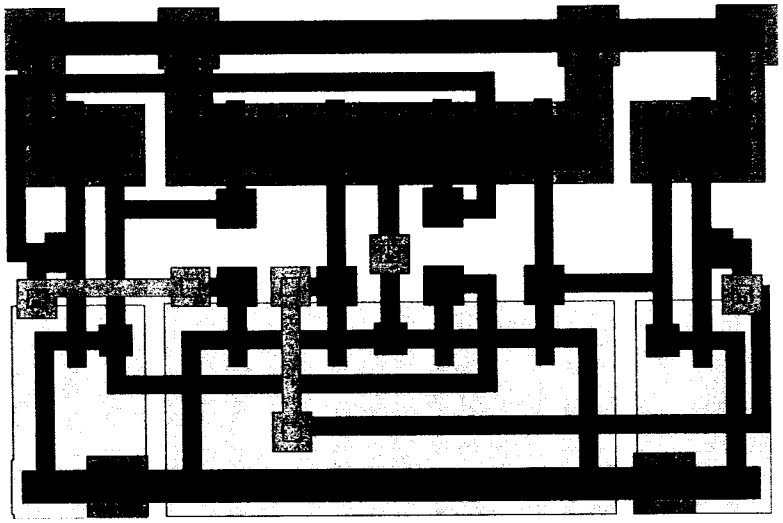
2. (4 marks) Create a 2-input CMOS NAND gate using CMOS3DLM technology in ELECTRIC based on the STICKS diagram from part (1) and include:
   a) Size the p-channel transistors three times "larger" than the n-channel transistors.

   Make sure your design passes DRC and functions correctly using the simulator built into ELECTRIC. Hand in a printout of your cell.

   Note: To print your cell, make sure the layout view is selected. Under "File | Print Options", select "Color". Use "File | Print" to print out your cell. Note that you can only print to a PostScript enabled printer. Turn off layers P-Guard, N-Guard, P+Mask, and N+Mask before printing for a cleaner image.

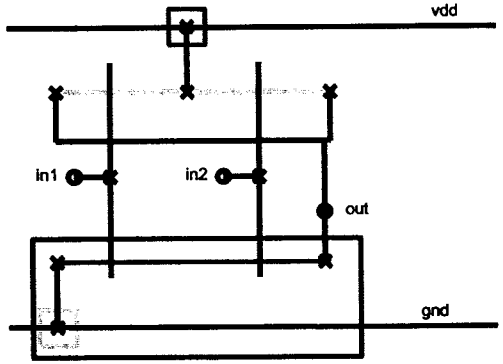
"I'm probably convincing you to drop math and go into carpet sales."

3. (4 marks) Being able to "reverse engineer" the layout of a facet (cell) is an important skill to verify the functionality of the cell as well as to uncover any layout errors.
   a) Identify the various layers by colouring the layers. Use the colours specified in question #1. If you need to use additional or different colours, make sure to provide a legend on your diagram.
   b) Draw the equivalent transistor level schematic for the circuit.
   c) What function does this cell provide?
   d) What <u>two</u> things are missing from the layout?



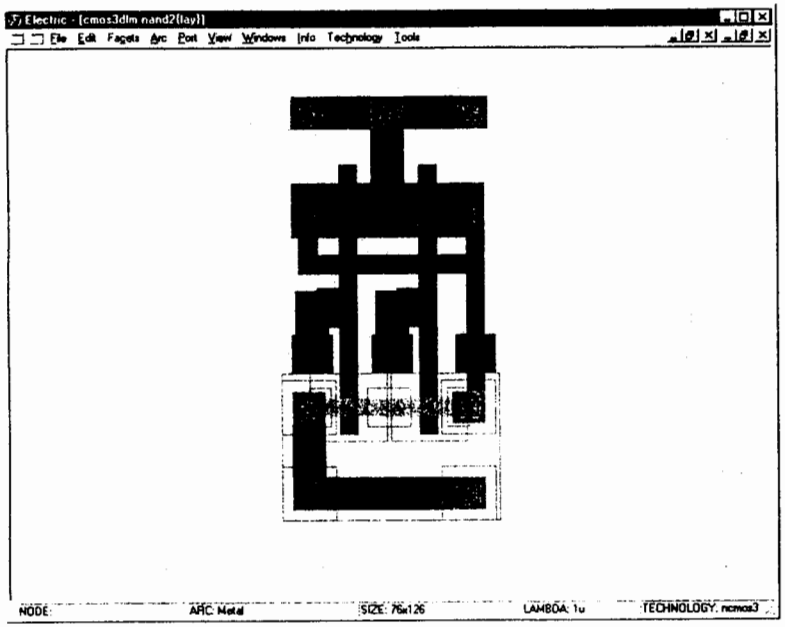
EE 451 / ENEL 489
Assignment # 2 SOLUTION

1. (2 marks) Create a "STICKS" diagram of a 2-input CMOS NAND gate:



2. (4 marks) Create a 2-input CMOS NAND gate using CMOS3DLM technology in ELECTRIC based on the STICKS diagram from part (1) and include:

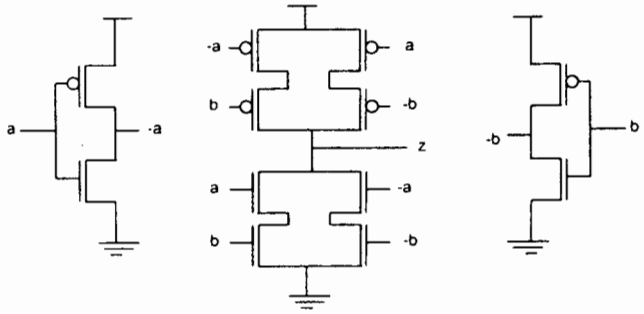
   a) Size the p-channel transistors three times "larger" than the n-channel transistors.



3. (4 marks) Being able to "reverse engineer" the layout of a facet (cell) is an important skill to verify the functionality of the cell as well as to uncover any layout errors.

   a) Identify the various layers by colouring the layers. Use the colours specified in question #1. If you need to use additional or different colours, make sure to provide a legend on your diagram.

   b) Draw the equivalent transistor level schematic for the circuit.



   c) What function does this cell provide?

   XOR

   d) What <u>two</u> things are missing from the layout?

   - Substate contacts to vdd.
   - P-well contact to gnd for middle p-well.

[Prof] "Say we had a class of 20 boys and 30 girls."
[Student] "So it's not an Engineering class."
[Prof] "umm... no."

EE 451 / ENEL 489
Assignment # 3 - Logic
Due: Thursday March 2, 2000

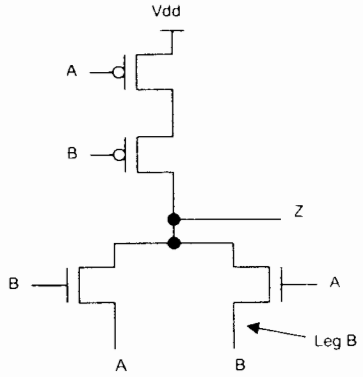
1. (4 marks) Given the function: $Z = (\overline{A} \cdot \overline{B}) + (C \cdot \overline{D})$

   a) Using INVERTERS, ANDs, and ORs, show a schematic of a circuit that performs this function. Assuming the gates are constructed using CMOS static logic, how many transistors would this circuit require?

   b) Reduce the equation using Boolean reduction into a form that is more suitable for implementing using INVERTERS, NANDs, and NORs Show the schematic of the circuit. How many transistors are required now (Hint: should be less than part (a))?

   c) Show the schematic of a CMOS static logic gate composed of eight transistors that performs the function Z.

2. (3 marks) Given the following schematic:

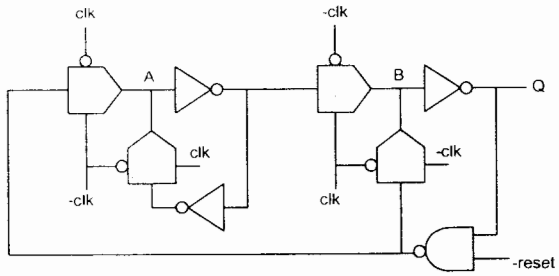


   a) Show the truth table for inputs A and B, and output Z.

   b) What function is this gate performing?

   c) Typically to completely test a combinational logic gate, one need only apply each of the possible input vectors. For a two input gate, there are only four possible combinations of inputs. If "Leg B" was an open circuit due to a manufacturing fault, show one sequence of the four input vectors that would **not** uncover the defect and show a second sequence of the four input vectors that **would** uncover the defect.

3. (3 marks) Given the following sequential logic circuit:



   a) Assuming A and B both start "low", show the waveforms for A, B, Q, and clk for four clock cycles of clk. What function is this circuit performing?

   b) Examine the reset signal "-reset". When does it correctly reset the circuit (i.e., force Q low) and when does it **not** correctly reset the circuit?

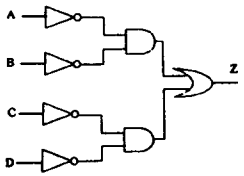
   c) How can the circuit be modified to as to provide a fully asynchronous reset?

Assignment #3
Solution

Question 1:

a) Use Inverters, Ands, and Ors:

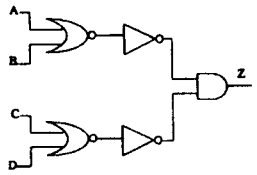
$Z=(\overline{A}\cdot\overline{B}) + (\overline{C}\cdot\overline{D})$



trans = (4 x 2) + (3 x 6) = 26

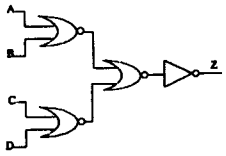
b) Reduce equation:

$$Z=\overline{(\overline{A}\cdot\overline{B}) + (\overline{C}\cdot\overline{D})} = \overline{(\overline{A}\cdot\overline{B})}\cdot\overline{(\overline{C}\cdot\overline{D})} = (A+B)\cdot(C+D)$$



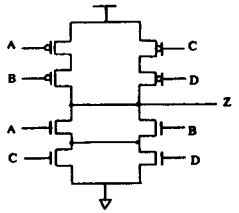
trans = (3x4) + (2 x 2) = 16

or: $Z = \overline{(A+B)} + \overline{(C+D)}$



trans = (3x4) + (1x2) = 14

c) 8-transistor version:



Question 2:

a)

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	1

b) This is an XNOR gate.

d) Sequence that would NOT uncover fault:

A	B	
0	0	
0	1	i.e., any sequence where a zero output
1	0	(e.g., A=0, B=1) proceeds A=1, B=0.
2	1	

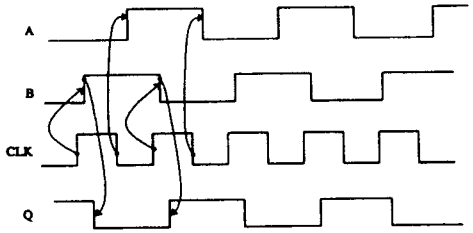
Sequence that would uncover fault:

A	B	
0	0	
1	0	i.e., any sequence where a one output
0	1	(e.g., A=0, B=0) proceeds A=1, B=0.
2	1	

"Pancakes are better than nothing, and nothing is better than love, therefore pancakes are better than love."

Question 3:

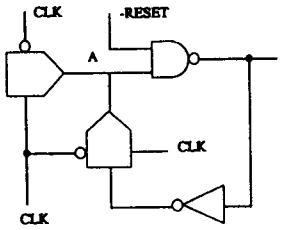
a)



Function is "divide by two"

b) Reset works correctly when CLK=0,
Reset does NOT work correctly when CLK=1.

c) To get a full asynchronous reset, replace inverter from A with NAND.



"And then I discovered the World Wide Web, and I said, 'Hey, this is neat. Look at all the pornography on it!'..."