UNIVERSITY OF SASKATCHEWAN
MIDTERM EXAMINATION

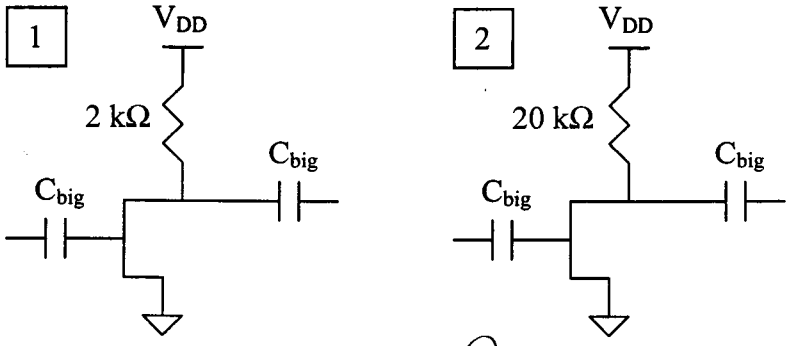
EE 457.3 Communications Electronics

Professor: Dr. D. M. Klymyshyn October 23, 2001
Time: **1.5 hours**
Notes: Exam is **closed book**. 1 page of formulas is allowed.
All questions are of equal value.

---

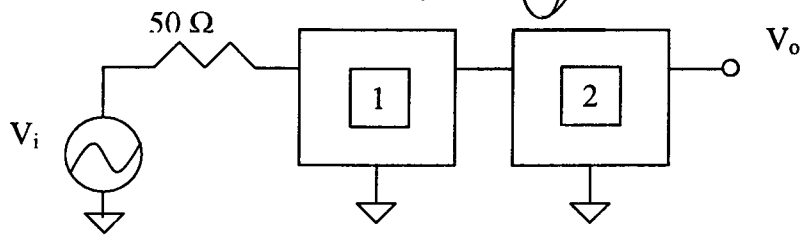
1. Design 2-element reactive L-type matching circuits to match a load impedance of $Z_L = 300 + j500\ \Omega$ to a source impedance of $Z_S = 100\ \Omega$. Estimate the Q of the matching circuits and choose the matching circuit with the **highest** Q.

2. Two small signal amplifier stages (identical FETs) are shown below (complete biasing circuitry is not shown). Estimate the 3 dB bandwidth of the cascade of the two sections, using configurations *A* and *B* as shown below. Which configuration, *A* or *B*, has higher frequency operation?

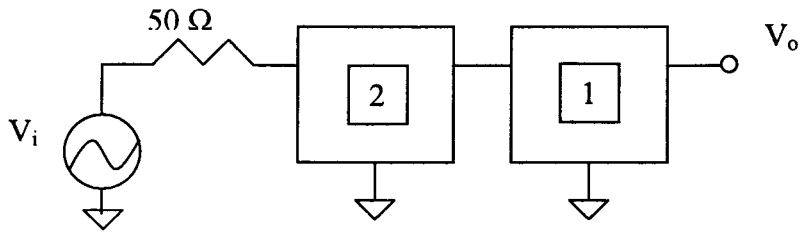


$C_{gs} = 3$ pF
$C_{gd} = 2$ pF
$C_{ds} = 2$ pF
$r_{ds} = 100$ kΩ
$g_m = 10^{-3}$ S

Configuration A



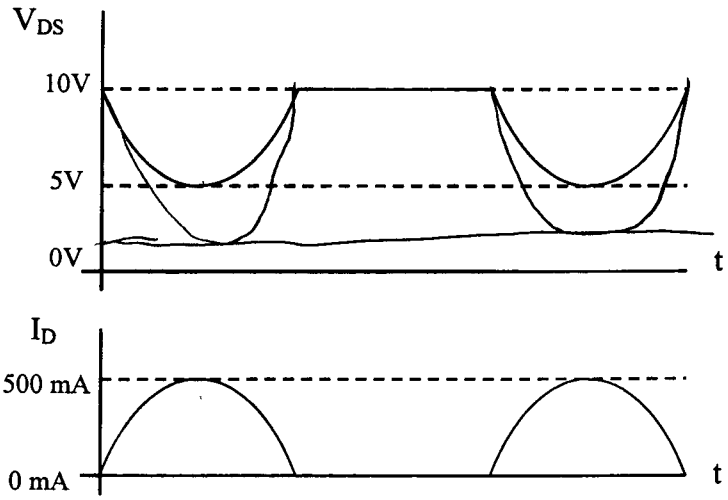
Configuration B

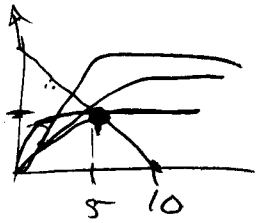


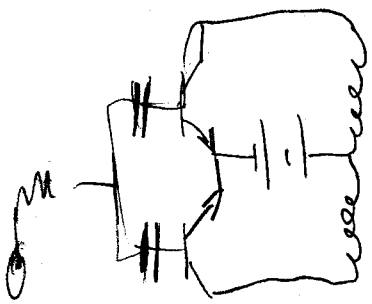
3. The waveforms at the drain of **one transistor** of a Class B **push-pull** power stage are shown below (the waveforms at the drain of the other transistor look the same but are 180 degrees out of phase).

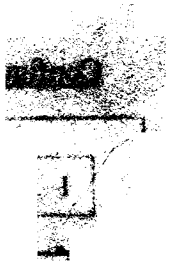
a. What is the load resistance seen by the drain? 10Ω
b. What is the **total** output power and power efficiency of the push-pull stage for the waveforms shown? 2.5W / 78.5%
c. What is the **maximum** output power and efficiency assuming V_{SAT} = 2 V? What do you have to change to obtain this? **Sketch the drain waveforms for this case.** (assume that $I_{d,max} = I_{DSS}$ = 500 mA, and that V_{DD} **cannot** be changed)

78.5%
$P_o = 3.125W$
$R_l' = 16\Omega$









c)