First IEEE International High Speed Interconnects Symposium
From Silicon to Systems

Program Abstracts

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Sponsored by IEEE UTD, IEEE CASS Dallas Chapter and SRC
First IEEE International High Speed Interconnects Symposium
From Silicon to Systems
UTD-TI Auditorium, Richardson, TX

Interconnects Continuum Paradigm and Benefits
Nagaraj NS
General Chair’s Message

The fascinating field of interconnects span from the trenches of ultra-deep-submicron silicon technologies to millimeter to kilometers of interconnects in systems. The fundamentals of Electromagnetics developed over 150 years ago govern the operations in the whole spectrum, while the adaptations of techniques are different at different levels. In the Interconnect Continuum paradigm, global optimization of interconnects for overall silicon to system performance and cost benefits can be achieved, circumventing local minima. This symposium covers several topics from silicon manufacturing, variability, SoC design, package/board design, reliability effects and emerging interconnects by eminent speakers in academia and semiconductor industry.

Biography

Nagaraj NS has been passionate about the field of interconnects for the past 25 years. He was drawn to Electromagnetics in his undergraduate degree in Electronics and Communications at UVCE, Bangalore and wrote a book on Electromagnetic Theory and Applications. After joining Texas Instruments in India in 1990, he completed MS in Software Systems at BITS, Pilani in 1992, focusing on analog circuit optimization and interconnects performance modeling. While working at TI-Dallas, he completed Ph.D. at UT-Dallas in 2003 in the field of Interconnects Signal Integrity and Reliability under the advice of Dr. Poras Balsara, Dr. Cyrus Cantrell and Dr. Dinesh Bhatia.

While at TI, for over two decades, he championed interconnect modeling and analysis, variability design techniques, product performance & power optimization and silicon closure. The innovations he pioneered have been applied on flagship products at TI including DSPs, ASIC and networking products and silicon closure techniques are implemented on digital products at TI. He has also contributed to several methods on library IP development, variation analysis, and package co-design and system level optimization. He championed Interconnect Symposium at TI (previously called Hot Interconnect) for over 17 years.

Nagaraj received Outstanding Contribution Award from SEMATECH for his industry-wide impact in Deep Sub-micron design methods and tools for parasitic extraction and signal integrity and for contributing to ITRS roadmap. He has 16 granted USA patents, more than 40 publications besides keynote speeches, invited talks and panel discussions in IEEE international conferences. He has co-chaired IEEE international workshops on Interconnect Design & Variability and Design for Manufacturing & Yield. He has mentored more than 10 SRC projects, students and several engineers at TI. Nagaraj has helped four startups launch and become successful.

To add to strong technical background, he has been pursuing EMBA at UT-Dallas focusing on Global Leadership, Innovation and Entrepreneurship and is a recipient of the Dean’s Excellence Scholarship Award. In pursuit of ‘success to significance’, he recently co-founded a Global Education Foundation in memory of his father to help develop the spirit of ‘Education is the best form of wealth’ (from an ancient Sanskrit poem).

Sponsored by IEEE UTD, IEEE CASS Dallas Chapter and SRC
Opening Speech

Cyrus D. Cantrell, Ph.D., P.E.
Erik Jonsson School of Engineering and Computer Science
University of Texas at Dallas

Abstract

This brief talk will open the First IEEE International High Speed Interconnects Symposium with a short historical perspective on the fundamental importance of interconnect issues and an overview of the Erik Jonsson School.

Biography

Cyrus D. Cantrell received the A.B. degree cum laude in Physics at Harvard University in 1962, the Master of Arts in Physics at Princeton University in 1964 and the Ph.D. in Physics at Princeton University in 1968. He is currently Professor of Electrical Engineering and Physics and Senior Associate Dean for Academic Affairs, Erik Jonsson School of Engineering and Computer Science at the University of Texas at Dallas.

Dr. Cantrell is a Life Fellow of the IEEE and the American Physical Society, and a Fellow of the Optical Society of America. He is licensed as a Professional Engineer in the State of Texas. In 2000 he was awarded the IEEE Third Millennium Medal. He has supervised and graduated 32 Ph.D. students.

Dr. Cantrell’s research areas are optical physics and the engineering applications of optical physics and electromagnetics. During a 6 ½ year period at Los Alamos National Laboratory, his work concerned the applications of optical physics to the separation of isotopes using lasers. At UT Dallas, he has supervised numerous doctoral dissertations on optical physics and its applications, and has also supervised or co-supervised dissertations on selected problems of computer architecture and interconnect modeling.
Keynote Speech

Inductance Influence in High Speed Design and Evolution of (PEEC) Partial Element Equivalent Circuit Techniques

Albert E. Ruehli
EMC Dept., Missouri U. of Science and Technology
Emeritus IBM Research, Yorktown Heights, NY

Abstract

Two basic themes are considered in this presentation: historical aspects of electrical interconnect modeling; and package modeling, with some examples of the problems as well as the evolution of solution approaches. The Partial Element Equivalent Circuit (PEEC) technique is a modeling technique which has evolved over several decades and is suitable for the 3D electromagnetic modeling of interconnects. We specifically consider some details for inductance computations and important aspects of electromagnetic modeling like 3D skin-effects.

Biography

ALBERT E. RUEHLI received his Ph.D. degree in Electrical Engineering in 1972 from the University of Vermont, Burlington, and an honorary doctorate in 2007 from the Lulea University in Sweden.

He has been a member of various projects with IBM including mathematical analysis, semiconductor circuits and devices modeling, and as manager of a VLSI design and CAD group. Since 1972, he has been at IBM’s T.J. Watson Research Center in Yorktown Heights, New York, where he was a Research Staff Member in the Electromagnetic Analysis Group. He is now an Emeritus of IBM Research and an adjunct professor in the EMC area at the Missouri U. of Science & Technology. He is the editor of two books, Circuit Analysis, Simulation and Design (New York, North Holland 1986, 1987) and he is an author or coauthor of over 200 technical papers.

Dr. Ruehli has served in numerous capacities for the IEEE. In 1984 and 1985, he was the Technical and General Chairman, respectively, of the ICCD International Conference. He has been a member of the IEEE ADCOM for the Circuit and System Society and an associate editor for the Trans. on Computer-Aided Design. He has given talks at universities including keynote addresses and tutorials at conferences, and has organized many sessions. He received IBM Research Division or IBM Outstanding Contribution Awards in 1975, 1978, 1982, 1995 and 2000. In 1982, he received the Guillemin-Cauer Prize Award for his work on waveform relaxation, and in 1999, he received a Golden Jubilee Medal, both from the IEEE CAS Society. In 2001, he received a Certificate of Achievement from the IEEE EMC society for inductance concepts and the Partial Element Equivalent Circuit (PEEC) method. He received the 2005 Richard R Stoddart Award, and in 2007 he received the Honorary Life Member Award from the IEEE Electromagnetic Compatibility Society for outstanding technical performance. In 2010 he received a best paper award at the EPEPS conference for his work on optimized waveform relaxation. He is a Life Fellow of the IEEE and a member of SIAM.
Keynote Speech

Performance Limitations of Cu/low-κ Interconnects and Possible Alternatives

Krishna Saraswat
Department of Electrical Engineering, Stanford University, Stanford, CA 94305

Abstract

For more than 30 years, the performance of silicon integrated circuits has improved at an astonishing rate. However, looking into the future the relentless scaling paradigm is threatened by fundamental limits including excessive power dissipation, insufficient communication bandwidth, and signal latency for both off-chip and on-chip application. Many of these obstacles stem from the physical limitation of Cu-based electrical wires, making it imperative to examine alternate interconnect schemes for future. This is further exacerbated by the increase in copper resistivity, as wire dimensions and grain size become comparable to the bulk mean free path of electrons in copper (~40nm). The paradigm shift toward multi-cores would require many longer global interconnects to communicate between cores, thus global wires would have to be pipelined deeper, in turn, latency becomes further worse. In this talk we examine the limits of Cu/low-k interconnects and explore possible advantages of two most important novel potential candidates: carbon nanotube based interconnects and optical interconnect. A review of recent results on heterogeneous integration of Ge optoelectronic devices for on- and off-chip optical interconnects will be done.

Biography

Krishna Saraswat received Ph.D. in Electrical Engineering from Stanford University in 1974. He is Rickey/Nielsen Chair Professor in the School of Engineering, Professor of Electrical Engineering and by courtesy Professor of Materials Science & Engineering at Stanford University. His research interests are in new and innovative materials, structures, and process technology of silicon, germanium and III-V devices and interconnects for VLSI and nanoelectronics. Areas of his current interest are: new device structures to continue scaling MOS transistors, DRAMs and flash memories to nanometer regime, 3-dimensional ICs with multiple layers of heterogeneous devices, ultrathin MOS gate dielectrics, metal and optical interconnections, and high efficiency and low cost solar cells. He has graduated more than 75 doctoral students and has authored or co-authored over 700 technical papers. He is a Fellow of the IEEE. He received the Thomas Callinan Award from The Electrochemical Society in 2000 for his contributions to the dielectric science and technology, the 2004 IEEE Andrew Grove Award for seminal contributions to silicon process technology, Inventor Recognition Award from MARCO/FCRP in 2007, the Technovisionary Award from the India Semiconductor Association in 2007 and the SIA Researcher of the Year Award in 2012. He is listed by ISI as one of the 250 Highly Cited Authors in his field.
Interconnect Manufacturing Challenges for the Most Advanced Technology Nodes

Andrzej J. Strojwas

Chief Technologist, PDF Solutions, Inc., San Jose, CA
Keithley Professor of ECE, Carnegie Mellon University, Pittsburgh, PA, USA

Abstract

Interconnect scaling has a very important effect on the overall chip size and has been as challenging as the new transistor architecture development. There have been many creative developments in both Middle of Line (MOL) and Back End of Line (BEOL) interconnect structures resulting in new local interconnect structures as well as application of double patterning starting from 20nm node. In this talk we will review manufacturing challenges facing the IC fabless and foundry companies for the 20nm nodes and below. In this talk we will focus on the IP design for manufacturability (DFM) aspects of double patterning as well as yield and reliability challenges ranging from printability, overlay/misalignment to defectivity issues. We will support the talk by real life examples from the state-of-the-art fabrication processes.

Biography

ANDRZEJ J. STROJWAS is Joseph F. and Nancy Keithley Professor of Electrical and Computer Engineering at Carnegie Mellon University. Since 1997 he has served as Chief Technologist at PDF Solutions, Inc. He has held positions at Harris Semiconductor Co., AT&T Bell Laboratories, Texas Instruments, NEC, HITACHI, SEMATECH, KLA-Tencor and PDF Solutions, Inc. He received multiple awards for the best papers published in the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Semiconductor Manufacturing and IEEE-ACM Design Automation Conference. He is also a recipient of the SRC Inventor Recognition Award. He was the Editor of the IEEE Transactions on CAD of ICAS from 1987 to 1989. He served as Technical Program Chairman of the 1988 ICCAD and Conference Chairman of the 1989 ICCAD. In 1990 he was elected IEEE Fellow.
Modeling and Layout Optimization for Robust 3D-IC Integration with TSVs

David Z. Pan
Department of Electrical and Computer Engineering
The University of Texas at Austin, TX 78712

Abstract

The 3D IC integration using through-silicon-vias (TSV) has gained tremendous momentum recently for industry adoption. However, as TSV involves disruptive manufacturing technologies, new modeling and design techniques need to be developed for robust 3D IC integration. In particular, TSVs in 3D IC may cause significant thermal mechanical stress, which not only results in systematic mobility/performance variations, but also leads to mechanical reliability concerns such as cracking. Meanwhile, the huge dimensional gaps between TSV, on-chip wires, and bonding-packaging lead to new electromigration concerns. Thus full-chip/package modeling and physical design tools need to be developed to achieve more reliable 3D IC integration. In this talk, we will discuss modeling and layout optimization issues for robust TSV-based 3D IC integration.

Biography

David Z. Pan received his Ph.D. in computer science from UCLA in 2000. He was a Research Staff Member at IBM T. J. Watson Research Center from 2000 to 2003. Since 2003, he has been with the Department of Electrical and Computer Engineering, UT Austin. He has published over 175 refereed journal and conference papers. He has served as an Associate Editor for IEEE Transactions on CAD, IEEE Transactions on VLSI, IEEE Transactions on CAS - I & II, IEEE CAS Society Newsletter. He has served as Chair of the IEEE CANDE Committee and the ACM/SIGDA Physical Design Technical Committee, Program/General Chair of ISPD, TPC Subcommittee Chair for DAC, ICCAD, ASPDAC, ISLPED, ICCD, ISCAS, and so on. He is a working group member of the International Technology Roadmap for Semiconductor (ITRS).

He has received a number of awards, including ACM/SIGDA Outstanding New Faculty Award (2005), NSF CAREER Award (2007), SRC Inventor Recognition Award three times, IBM Faculty Award four times, UCLA Engineering Distinguished Young Alumnus Award (2009), 9 Best Paper Awards (ASPDAC 2012, ASPDAC 2011, IBM Research 2010 Pat Goldberg Memorial Best Paper Award in CS/EE/Math, ASPDAC 2010, DATE 2009, ICICDT 2009, SRC Techcon in 1998, 2007 and 2012), Communications of the ACM Research Highlights (2013), ISPD Routing Contest Awards (2007), eASIC Placement Contest Grand Prize (2009), ICCAD’12 CAD Contest Award, among others. He was an IEEE CAS Society Distinguished Lecturer for 2008–2009.
Meeting the Signal Integrity Challenges of High-Speed Interconnects and Systems

Dr. Ram Achar, Ph. D., P. Eng.,
IEEE Fellow
Professor, Department of Electronics,
Carleton University, Ottawa, Ontario - K1S 5B6
Email: achar@doe.carleton.ca
Ph: 613-520-5651, Fax: 613-520-5708

Abstract

With increasing demands for high signal speeds coupled with decreasing feature sizes, interconnect effects such as signal delay, distortion and crosstalk become the dominant factors limiting the performance of high-speed systems. On the other hand, interconnect structures can be diverse and present at any of the hierarchical packaging levels including integrated circuits, printed circuit boards, multi-chip modules and backplanes. Addressing the high-frequency signal integrity issues and managing the complexity of high-speed designs is becoming increasingly critical.

In this talk, high-frequency, system level and co-performance issues of signal integrity will be discussed. Advanced signal integrity modeling/simulation strategies applicable to various levels of system hierarchy will be described. Particular emphasis will be placed on distributed, long and large coupled interconnects as well as high-frequency current distribution related effects, such as skin, proximity and edge effects will be considered. Diverse applications covering wide spectrum of on-chip, multichip, packages, printed circuit boards, backplanes/connectors will be considered.

Biography

Prof. Achar is an active researcher contributing to the advancement of computer-aided design tools and methodologies for analysis of high-frequency circuits and systems. He has published over 180 peer-reviewed articles in international journals/conferences, six multimedia books on signal integrity and five chapters in different books. Dr. Achar currently is a professor of electronics engineering at Carleton University. Dr. Achar and his students received several prestigious awards, including the NSERC (Natural Science and Engineering Research Council) doctoral medal, Strategic Microelectronics Corporation (SMC) Award and Canadian Microelectronics Corporation (CMC) Award. He was also a co-recipient of the IEEE advanced packaging best transactions paper award (2007).

Dr. Achar currently is a guest editor of IEEE Transactions on CPMT, for special issues on “Variability Analysis” and “3D-ICS/Interconnects”. Previously, he served as the Distinguished Lecturer for the CAS society (2010, 2011), General Co-Chair EPEPS-2011 and as International Guest Faculty on the invitation of the Dept. of MCIT, Govt. of India, under the SMDP-II program. He also currently serves on the executive/steering/technical-program committees of several leading IEEE international conferences, such as EPEPS, EDAPS, ECTC, SPI, ASP-DAC, etc. and in the technical committees, EDMS (TC-12 of CPMT) and CAD (MTT-1). He is a founding faculty member of the Canada-India Center of Excellence, chair of the joint chapters of CAS/EDS/SSC societies of the IEEE Ottawa Section, and is a consultant for several leading industries focused on high-frequency circuits, systems and tools. Dr. Achar is a Fellow of IEEE. For more details, please visit: http://web.doe.carleton.ca/~achar/

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System Level ESD - Beyond the Component Level IC Protection

Charvaka Duvvury
Industry ESD Expert and Co-Chair of Industry ESD Council

Abstract

It is well known in the industry that ESD is always a challenging issue for IC reliability. In recent years the component level IC protection against ESD has seriously become a major challenge due to advanced scaling of silicon technologies and the development of complex high speed circuits including the effects of system on chip (SoC) applications. But ESD protection doesn’t end at the IC pin but is a system feature with much harsher requirements than on IC level. In addition to the necessary component level ESD protection for safe handling at the IC production areas, the system level ESD protection at the board level during end-user applications is becoming even more critical. IEC 61000-4-2 standard specifies ESD testing of complete system like a mobile as well as a car and is an inevitable feature. To account for this in a cost efficient manner a new printed circuit board (PCB) design methodology needs to be employed called system efficient ESD design (SEED) which involves electromagnetic compatibility design measures, software development and new types of PCB hardware testing. An understanding of coupling from the interface pins and cross-coupling between pins of different ICs on the board would be important for system level ESD protection designs. This seminar will address these important topics and give an insight into the strategies for coupling from component to system protection design. A roadmap for ESD and the need for innovative approaches that include advanced simulations will be reviewed.

Biography

Charvaka Duvvury was a Texas Instruments fellow while he worked in the Silicon Technology Development group. Charvaka is also a fellow of the IEEE. He is currently on Leave of Absence and working as a technical consultant on ESD design methods and ESD qualification support. Charvaka received his PhD in engineering science from the University of Toledo. After working as a post-doctoral fellow in physics at the University of Alberta in Canada, he joined Texas Instruments where he has worked for more than 35 years. Charvaka has made numerous international presentations on ESD phenomena and protection design. He has published over 140 papers in technical journals and conferences and holds more than 70 patents. He has co-authored books on ESD design (ESD In Silicon Integrated Circuits, John Wiley & Sons, 2nd Edition 2002), hot carriers, and modeling of electrical overstress. He is a recipient of the Outstanding Contributions Award from the EOS/ESD Symposium (1990), Outstanding Mentor Award twice from the SRC (1994 and 2012), and numerous best paper and best presentation awards from the EOS/ESD Symposium. He served as the General Chair for the ESD Symposium both in 1994 and in 2005. He was a contributing editor for the IEEE Transactions on Device and Materials Reliability (TDMR) from 2001-2011. Charvaka has been a member of the ESD Association board of directors since 1997, promoting university education and research in ESD. He is a co-founder and co-chair of the Industry Council on ESD Target Levels.
Interconnect Challenges in Large Scale Multicore Chips

Don Steiss
Cisco Design Systems
Richardson, TX

Abstract

In advanced chip fabrication technologies, interconnect characteristics are first-order considerations for architectural and micro-architectural decisions. This talk describes some of the issues and solutions in large scale multicore processor designs related to chip interconnect.

Biography

Don Steiss received the Bachelor of Engineering degree from Rose Hulman Institute of Technology in 1984 and the Masters of Engineering degree from the University of South Florida in 1986. Don worked for several years at Texas Instruments in high speed circuit and microprocessor development where he was a distinguished member of the technical staff. Since 2002, Don has worked at Cisco Systems, and is currently a Principal Engineer responsible for packet processor architectures for the Silicon Engineering group.
The Search for Negative Impacts of 3D Cu TSVs

Jeff West
Texas Instruments Inc.
Dallas, TX

Abstract

Some of the primary concerns about integrating Cu TSVs into CMOS logic include the impact to transistor performance resulting from TSV-processing induced back-side Cu contamination and front-side proximity stress. The impact of intentionally contaminating the wafer back-side with Cu was studied, as was the impact of 10x60um Via-Middle TSV proximity to 28nm CMOS poly-SiON P/NFET transistors. Intentional back-side Cu contamination was found to have no impact to any CMOS parameter measured. A proximity study (distance > 1.5um) determined that the impact of TSVs on strain-engineered transistors (<2.3%) is essentially negligible compared to other sources of variation in the process, such as that due to the context dependency of dual stress liner boundaries (~10%).

Biography

Jeff West has worked on technology development and transfer at Texas Instruments for 22 years. He is a Distinguished Member of the Technical Staff and holds 21 patents. In addition to leading TI’s efforts to integrate dual damascene Cu low-k interconnect into production in 2000, he led TI’s integration activity for embedding TSVs into logic devices, for which a functional Wide IO logic-memory interface was demonstrated for the first time in 2012. He currently works on high voltage isolation technology development. He served on the TI Technical Council for 6+ years and has been a member of TI’s SC Patent committee since 2008. He holds a Ph.D. in Materials Science from Harvard University.
Si2 Standards for 2.5D / 3D Design Flows

Sumit Dasgupta
Silicon Integration Initiative
Austin, TX

Abstract

This presentation describes the status of standards development at Si2 to support design flows for 2.5D and 3D packages. It provides an introduction to Si2 and its development process and how 2.5D / 3D standards fit into the overall direction of Si2.

Biography

Sumit DasGupta is Senior Vice-President of Engineering at Silicon Integration Initiative (Si2), a semiconductor industry consortium based in Austin, TX. Prior to joining Si2, Sumit was at Motorola Semiconductors, now Freescale, where he served as Director of Design Systems and was responsible for developing and integrating software tools for the design of PowerPC microprocessors and SoC’s. While at Motorola, Sumit served as a key member of the DAPIC group at Si2 which defined the technical, business and legal structure of the OpenAccess Coalition. Before Motorola, Sumit was at IBM where he served in senior management and technical leadership positions in the Electronic Design Automation (EDA) group and was responsible for developing design tools and methods for physical design, and design for test.

Sumit has a PhD in Computer Science from Syracuse University. He has 8 patents issued and over 25 papers and publications. He is a Senior Member of the IEEE and has served in several leadership positions in IEEE boards, events and activities.
Expanding the Design-Manufacturing Interface for 3D IC

Juan C. Rey
Mentor Graphics Corporation
San Jose, CA

Abstract

This talk covers the business trends and drivers for 3-D ICs. Issues related to 3-D design and manufacturing enablement are discussed in detail. Moving beyond the immediate challenges, challenges in advanced extraction and stress effects are discussed.

Biography

Juan C. Rey is the Senior Engineering Director for the Calibre product line in the Design to Silicon Division at Mentor Graphics Corporation; his group is responsible for the architecture, design and development of a software product line for integrated circuits physical verification and tape out tasks such as design rule checking, layout vs. schematic verification, capacitance, resistance and inductance extraction, resolution enhancement, mask data preparation and design for manufacturing. Juan has 30 years of software development experience ranging from research activities at Stanford University (EE department), to development and management of electronic design automation and process/device modeling software at Technology Modeling Associates, Cadence and Mentor Graphics. Juan also represents his company at the Executive Technology Advisory Board of Semiconductor Research Corporation (SRC) and is responsible for the IP portfolio and research initiatives of his division.
Power Integrity for Systems with High Speed Signals

Tingdong Zhou, and W. Dale Becker
IBM, Austin, TX and Poughkeepsie, NY

Abstract

The analysis of the power distribution network (PDN) in high-performance systems is a challenge for the design engineer presented with continually increasing technology. The era of smart computing enables big data and deep analytics which results in many high-speed signals in systems with relatively high power and high current density. New technology elements, such as 3D silicon and packaging, provide the opportunity for high compute density while creating a demanding PDN design and analysis. This presentation gives an overview of the PDN noise components, the impact on the circuits and signals within the system and discusses the modeling, simulation and analysis that is used to provide input to the designer. Some designs that mitigate PDN noise effect are also included.

Biography

Tingdong Zhou received the B.S.E.E. and M.S.E.E. degrees from Tsinghua University, Beijing, in 1992 and 1995, and the Ph. D. from the University of Arizona, Tucson, in 2002. He is a Senior Engineer in IBM System and Technology group. He has been working on the electrical design of multiple generations of IBM POWER servers and Z mainframes since 2002. His current interests focus on electromagnetic modeling of high-speed circuits, electrical modeling and simulation of high speed and high performance packages, and signal and power integrity issues in the design of server systems. He has published over 40 conference and journal papers and 12 patents.

Dale Becker received the B.E.E degree from the University of Minnesota, M.S.E.E. from Syracuse University and the Ph.D. from the University of Illinois at Urbana Champaign. He is a Distinguished Engineer in IBM Systems and Technology Group and a member of the IBM Academy of Technology. He is the System Electrical Architect for the IBM POWER and System Z Enterprise Systems. His responsibilities include designing the high-speed channels to enable the computer system performance and the power distribution networks for reliable operation of the integrated circuits that make up the processor subsystem. Dr. Becker has 25 patents on electrical design of computer systems and has presented 75 papers in refereed journals and international conferences covering many aspects of electrical computer system design including power distribution analysis and design and modeling of signal and power distribution networks. He is a senior member of IEEE, an iNEMI Technical Committee member and a member of IMAPS.

Sponsored by IEEE UTD, IEEE CASS Dallas Chapter and SRC
Design of High Speed Differential Links in IBM Servers

Rohan Mandrekar
Systems and Technology Group, IBM, Austin TX

Abstract

In advanced chip fabrication technologies, interconnect characteristics are first-order considerations for architectural and micro-architectural decisions. This talk describes some of the issues and solutions in large scale multicore processor designs related to chip interconnect. In recent years, high performance microprocessors have seen a sharp increase in the number of cores offered on a single microprocessor die. This increase in the number of cores has considerably increased the bandwidth requirements on the microprocessor interfaces. This is especially true in the case of high performance servers which need substantial memory bandwidth and high speed processor-to-processor links to enable multi-way systems. Such systems require very high density of packaging around the microprocessor. However, such dense packaging introduces several signal integrity issues that need to be considered carefully for the system to meet its target performance requirements. This talk discusses how these challenges can be addressed through a combination of modeling and measurement.

Biography

Rohan Mandrekar received his B.E (Electronics) degree from the University of Mumbai in 2001, and his M.S and Ph.D degrees (in Electrical Engineering) from the Georgia Institute of Technology in 2003 and 2006 respectively. His graduate research focused on the co-simulation of signal distribution and power delivery networks in high speed systems. At IBM, Rohan is a technical lead of the signal integrity team responsible for design and implementation of high speed processor interfaces for the IBM POWER platform. He is responsible for modeling and simulation activities that establish the electrical requirements for the next generation IO interfaces. He has co-authored over 25 publications in IEEE conferences and journals and is currently on the 3rd invention plateau at IBM. Rohan is a senior member of the IEEE and has served as the program co-chair and treasurer for the Austin IEEE CPMT chapter. He also serves as a reviewer for the IEEE Transactions on Components, Packaging and Manufacturing Technology.
System Co-design and optimization for high performance and low power SoC’s

Siva Kothamasu¹, Snehamay Sinha¹, Amit Brahme²
¹Texas Instruments Inc., Dallas, TX
²Texas Instruments India Pvt. Ltd., Bangalore, India

Abstract

With the ever increasing interface speeds and massive feature integration on the modern day SoC’s there has been an increased focus on Signal Integrity and Power Integrity design and analysis. There is also an increasing trend in shrinking feature sizes on the packages and Printed Circuit Boards. For a successful SoC design, it is important to understand the various interactions among Chip, Package and Printed Circuit Boards and optimize at the right place. Designing the Chip, Package and Printed Circuit Board together is commonly referred to as System Co-Design. In this talk, we introduce the concept of System Co-Design and present some practical design approaches to address these challenges.

Biography

Siva S Kothamasu is an elected Member Group Technical Staff at Texas Instruments, and works in the System Applications team, Embedded Processor group in Dallas. He is actively involved in System level Signal Integrity, Power Integrity issues/challenges working with several customers. He has led the Package Co-Design team working across several products in TI. He has more than 10+ years industry experience working in various aspects of chip design covering Reliability CAD, Physical Design, Signal/Power Integrity Analysis and Package Co-Design. He has several papers in internal and external forums and is a member of IEEE. He holds a Bachelor of Engineering degree from Osmania University.

Snehamay Sinha received the Ph.D. degree in Physics from Tata Institute of Fundamental Research in 1995. Since graduation he has been at Texas Instruments, first in Bangalore and then in Dallas. He has worked in many areas, starting with CAD tool development for full chip ESD and EM checking, then moving on the crosstalk and substrate noise analysis. Currently, he leads the System Co-design team in Dallas for the Processors group in TI where he dabbles in package design and signal and power integrity for high speed DSP SoC’s. He is one of the TI representatives in the Logic and Physical Design Technical Advisory Board at SRC. He has authored or co-authored multiple papers and holds 4 patents.

Amit Brahme received Bachelor of Engineering degree in Electronics & Telecommunication from University of Pune. Since graduation he has been working with Texas Instruments (India). He has worked in the area of reliability analysis and package/board co-design for the last decade. Currently he manages Package Co-design team in Processor group in TI India.