SYSTEM LEVEL ESD - BEYOND THE COMPONENT LEVEL IC PROTECTION

CHARVAKA DUVVURY
Outline

• Impact from Advanced Technologies and High Speed Circuit Designs on Component Level ESD
• System Level ESD and the coupling from component to System ESD design
• Simulations and Tools for efficient System Level ESD designs
• Future issues
Stages of ESD Protection Methods and Design

Component ESD

System level ESD

1. **Wafer**
   - **Fab environment**
     - Measure:
       - Ionizer
       - Static handling

2. **IC component**
   - **IC Assembly & Test**
     - Measure:
       - Grounding
       - Ionizer

3. **Board**
   - **Board assembly & repair**
     - Measure:
       - Systemlevel protection

4. **System**
   - **End customer operation**
     - Measure:
       - Shielding
       - Prerunning ground

**ESD Protected Area**
Human Body Model (HBM) Reduced from 2kV ➞ 1kV

Charged Device Model (CDM) Reduced from 500V ➞ 250V
• Closing of the ESD Design Window to <1kV HBM

• Severe impact also on CDM
IMPACT ON HIGH SPEED DESIGNS

- Data Rates are influenced by the ESD loading capacitance
- For >20 Gb/S, 2kV HBM and 500V CDM are not possible to achieve
- Capacitive loading of ESD protection for high speed serial (HSS) link design is limited to ~ 100 fF.
Protection for HBM/CDM

Commonly used for HSS designs

R1 is good for CDM but degrades data rates
Package and IO Speed Impact on CDM

Data Rates, Tech. Node and Package Size all will have impact on achievable CDM
Designing for 3D IC ESD protection is still evolving. ESD issues are a big unknown because any interactions through the TSV have not been clearly investigated. When stacking a die from another company may mean not enough information is known about the circuitry that touches TSV pillars.

Schulmeyer et al. SEMICON West 2012
Industry Council on ESD Target Levels
System Level ESD
System Level ESD

- **What is a System Level ESD Event?**
  - An electrical system experiences an ESD Event

- **What can happen in a System Level ESD Event?**
  - The system continues to work without problem
  - The system experiences upset/lockup, but no physical failure.
    - Typically referred to as “Soft Error”
    - May or may not require user intervention
  - The system experiences physical damage
    - Typically referred to as “Hard Failure”

The [IEC 61000-4-2](https://www.iec.ch) ESD Test Method is used to assess the robustness to system ESD events
ESD On Systems

Electric and magnetic fields produced by ESD couple to the system in multiple ways, causing failures.

The IEC 61000-4-2 Test Method is used to represent a changed human holding a metal object to discharge.
Waveforms of Component HBM and System Level

Discharge current thru a 2-Ohm load

Even 4 kV HBM is not same as 4 kV IEC!
There is no correlation between HBM and IEC
The requirements for IEC test are often 8kV
Differentiation of Internal Vs. External Pins

- All the external pins are stressed with the IEC pulses
- Interaction to the corresponding interface pins?
- What about cross-coupling?
Designing for the Overall System

System ESD protection design involves an understanding of the system, independent of component ESD levels.

EXTERNAL PROTECTION ON PCB
- Isolation Impedance
- Residual Pulse Current
- External Clamp (TVS)
- PCB Track
  - Bypass capacitor
  - Common Mode Filter
  - Chip Ferrite Bead
  - Isolation Resistor

INTERNAL PROTECTION ON IC
- Internal Clamp (IC’s ESD protection)

IEC Pulse +1-8 kV
- Stress Point
- Connector
- 30 A
- 30 ns → 60 ns
- t=0.7 to 1 ns

Industry Council 2013
For an efficient system protection design, the IC pin’s breakdown characteristics play a critical role.

Effective IEC protection design can be achieved for any IC pin that interfaces with the external world.
Evaluation Board (Reference Platform)

Smart Phone Application Board
Simulation Methodology (SEED)

IEC Stress

IEC Pulse

100-ns Pulse IV

Pulse IV

TLP Info

V

TLP Info

It2

100-ns

Power IC

CDM Info : Ip

TLP Info : It2

V(f)

TVS

Response to IEC Pulse

Residual Pulse from Board Design

Industry Council 2013

18
Simulated Current Waveform at IC pins

- Transient simulation
- +8kV IEC at D- Connector pin
- Additive contribution of each elements
- Suppression of the First IEC Peak by the PCB

Industry Council 2013
- EM simulation → [S] model
- Post CMF interconnect
  - Leq~30 nH / Req~0.9 Ω
  - Raise isolation impedance between TVS and IC
  - More effective to mitigate the first IEC peak (inductance)
Under an IEC event

- Insertion impedance defined by Load Mode
- Load formed by On-Chip/Off-Chip On Resistance (positive or negative to ground) and PCB interconnect

Industry Council 2013
Crosstalk to Internal Pins

Friedrich zur Nieden, Stanislav Scheier, Stephan Frei; „System level ESD on-PCB coupling”, report 2011.

Industry Council 2013

---

Table 1: Simulated quantities at CANH pin

<table>
<thead>
<tr>
<th>V_{charge} [kV]</th>
<th>V_{max} [V]</th>
<th>I_{max} [A]</th>
<th>E [fJ]</th>
<th>E/E_{1kV}</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>50.24</td>
<td>3.86</td>
<td>4.67</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>77.52</td>
<td>8.03</td>
<td>12.42</td>
<td>2.66</td>
</tr>
<tr>
<td>4</td>
<td>132.01</td>
<td>16.36</td>
<td>35.99</td>
<td>7.71</td>
</tr>
<tr>
<td>8</td>
<td>240.90</td>
<td>32.96</td>
<td>115.51</td>
<td>24.73</td>
</tr>
</tbody>
</table>

Table 2: Simulated quantities at µC DATA pin

<table>
<thead>
<tr>
<th>V_{charge} [kV]</th>
<th>V_{max} [V]</th>
<th>I_{max} [A]</th>
<th>E [fJ]</th>
<th>E/E_{1kV}</th>
<th>Energy Coupling Factor (E_{N4}/E_{N4})</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.98</td>
<td>0.08</td>
<td>0.28</td>
<td>1</td>
<td>16679</td>
</tr>
<tr>
<td>2</td>
<td>3.02</td>
<td>0.09</td>
<td>0.29</td>
<td>1.06</td>
<td>42828</td>
</tr>
<tr>
<td>4</td>
<td>3.08</td>
<td>0.11</td>
<td>0.37</td>
<td>1.34</td>
<td>97270</td>
</tr>
<tr>
<td>8</td>
<td>3.18</td>
<td>0.16</td>
<td>0.68</td>
<td>2.46</td>
<td>169870</td>
</tr>
</tbody>
</table>

---

Graphs showing voltage and current waveforms for different input conditions.
Extended SEED

Basic SEED
Conducted discharge leads to damage

Extended SEED
Covers also soft fails due to low injected currents and EM radiation
Discharge via wired network connected to PCB port

(A) ESD and EMI energy spread deep into the system, potentially creating secondary problems.

(B) ESD and EMI energy guided out of the system as soon as possible, keeping "noisy" and "quiet" areas isolated. Best practice.

(C) ESD and EMI energy primarily filtered at the system periphery. Some residual noise/energy continues on inside, but the level is reduced and does not create additional secondary issues. Best cost/performance tradeoff.

Off-Chip Protection is the ideal approach
Industry Council 2013
SEED Categories

SEED Category 1:
a) External pin experiences hard failure due to a direct ESD zap (failure root cause: high pulse energy at exposed line) OR
b) Non-external pin experiences a hard failure due to an indirect ESD zap (failure root cause: high transferred pulse energy to non-exposed lines)

SEED Category 2: Pin experiences a transient latch-up event which can lead to either a hard or soft failure (failure root cause: current injection into the substrate which is too high)

SEED Category 3: Describes protection of an IC experiencing soft failure due to low amplitude transient bursts in the system during an ESD zap (for example, this may be caused by degraded signal integrity of an exposed line or cross-talk to a neighboring line or supply noise).
Technology Trends

• New technology directions for both IC designs and applications will start to have impact on how well system level ESD designs can be done

• The impact is from
  – ICs and Microprocessors
  – Automotive Applications
  – IC Packages and Applications
  – Advances in Board Assembly/Technologies
  – Optical Interconnects
  – New Polymer Materials
  – Compatibility to IEC Protection Requirements
DSP and Microprocessors

• SerDes: 20 GB/sec at 20nm - Internal
• DDR:2.3G at 28nm - Internal
• USB and HDMI - External
• RF Antenna low tolerance to capacitance - External

The external pins require special attention for all future system level ESD designs

Industry Council 2013
USB Roadmap Projections

- **USB1**: 1995, 12MB/sec, 130nm
- **USB1.1**: 2001, 48MB/sec, 90nm
- **USB2**: 2004, 480MB/sec, 65nm to 28nm
- **USB3**: 2011, 5GB/sec, 28nm

Increasing challenges for IEC Protection

- **5V** to **3.3V** to **1.8V**

Includes compatible port for UBS2

Industry Council 2011
HDMI Projections

Increasing challenges for IEC Protection

2005

- Composite
- S-Video

<100MB/sec

65nm

2008

1.8GB/sec

32nm

2011

2.4GB/sec

28nm

2012

>3.4GB/sec

28nm

2015

5.4GB/sec

28nm

Display Ports

Industry Council 2011
Automotive Trends

• **High integration**, such as System Base Chips, system ASICs - next 5 years technology feature in the sub-100nm range. The chip area required for system level ESD protection is not able to shrink

• **Integrated sensor technologies** - for the coming years is an increase of logic density and signal bandwidth

• **Microcontroller technologies** - In the next years system level robustness will be required for certain pins (GPIO, ADC inputs) with external PCB-level protection measures.
Package Trends

• System-in-Package (SiP) needs to carefully match all IC and product interfaces - includes EMC/ESD compatibility issues

• The same IC may contain digital, analog and RF blocks.

• May not be possible to separate noisy RF interfaces on a board from other sensitive interfaces

• For higher board integration more detailed information is needed from Systems on Chip blocks and most likely early EMC/ESD simulations are needed to optimize design
3D IC ESD/EMI Effects

• For stacked die packages, the complexity for ESD increases
• The dominant effect on EMI is the interposer design and die to die coupling
• A basic EMC design rule is to guide the ESD/EMI out of the component as soon as possible.
• Going into future applications of die stacking, these effects could dominate the design of system level ESD.
PCB Trends

- Board 3D design with stacked components, embedded components in PCB, System-in-Packages, System-on-Packages and other 3D constructions
Conclusions

• Component level ESD is not a major issue as long as minimum safe levels for HBM and CDM are maintained
• For system level ESD on-chip solutions are challenging and are not efficient
• For interface pins external protection is optimum as long as the board designs take into consideration the response of the external TVS and the I/O pin’s transient characteristics
• As technologies advance there will be many challenges for meeting system level ESD requirements
Acknowledgments

• Dr. Harald Gossner – Intel Mobile Communications
• Industry Council on ESD Target Levels

References

JEDEC Documents:
JEP155 and JEP157 (HBM and CDM)
JEP161 and JEP162 (System Level ESD)