Si2 Standards for 2.5D / 3D Design Flows

Sumit DasGupta, PhD
Sr. Vice President, Engineering
Silicon Integration Initiative (Si2)
Austin, TX 78759
Email: dasgupta@si2.org
About Si2

• Non-profit, chartered in 1988 under the U.S. NCRPA
  – Benefit includes unique IP legal protections / safety
  – Global mission, charter, bylaws

• Headquarters: Austin, TX, USA

• Over 85 corporate members worldwide
  – Largest standards org chartered in IC design / manufacturing
  – Plus numerous industry & research partnerships

• Si2 website statistics
  – ~23,000 hits/day
  – >6,700 members and associates
  – >75,000 Si2 site downloads
    • >32,000 OpenAccess downloads
Si2 Standards Development Process

- Project Proposal Creation / Market Analysis
- Project Approval from Si2 Board
- Project Kick-Off / Membership Drive
- Release RFT / Receive Contributions
- Create Project Plans / Evaluate Contributions
- Create / Approve Standard Specs
- Legal Clearance for Standard Specs
- Develop Adoption Collateral for Members **
- Release Standards to Industry

** For coalitions only
Design Flow Standards For 2.5D / 3D

- 2.5D / 3D Planning
  - Architecture Planning
  - Physical Planning
  - Package Planning

- 3rd Party Die IP
- PCB Design

- Die / Interposer Design
  - Logical Design
  - Physical Design
  - Logical /Physical/Electrical Verification

- Physical Integration
  - Logical /Physical/Electrical Verification

- Stack / Interposer Integration

Si2 Standardization Areas

4/30/2013

Innovation Through Collaboration
2.5D / 3D Design Flow Standards

2.5D / 3D Planning
- Architecture Planning
- Physical Planning
- Package Planning

Multi-die thermal estimation

Multi-Tier Die / Interposer Design / Mfg
- 3D PDK
- Electrical Design / Verif
- Physical Design / Verif
- Thermal Mech Analysis
- Chip Finishing, Extraction, DRC, LVS

Multi-die power networks

Multi-die parasitic networks

Electrical Design / Verif

Physical Design / Verif

Thermal Mech Analysis

Chip Finishing, Extraction, DRC, LVS

Mask Creation, DFM, Data Prep

Foundry

Partitioning

TSV, interposer properties

3rd Party Die IP

RLC models, RDL layers, u-bumps

API between EDA, T/M tools

DFT / ATPG constraints

Partitioning / FP & DFT constraints

Thermo-mech. corner conditions

Packaging & Test

Stack Integration

3rd Party Die IP

Chip-Chip & Chip-Package Desc

4/30/2013

Innovation Through Collaboration
Open3D Project Details

- **Scope**: Enable interoperable 2.5D / 3D design flows based on open standards to facilitate exchange of relevant design information
  - Define open interfaces (API’s & file formats)
  - Full IP / legal protection
    - No risk to proprietary algorithms, products, or methodologies
- **Process**: Stage project over multiple phases, focusing on most urgent items first:
  - Phase 1: Design exchange formats / API’s and sub-flows
    - Examples include formats for:
      - 2.5D / 3D partitioning and floorplanning information for design of tiers
      - Tier-2-tier (& interposer) constraints due to thermal distribution, mechanical stress, exclusion zones for bumps, etc.
  - Phase 2: Model exchange formats / API’s and sub-flows
    - Examples include formats for electrical models, thermal / mechanical stress models, etc.
  - Phase 3: Format / API standards for full 2.5D / 3D design flows
- **Membership**: Include companies from 2.5D & 3D space and domain experts from academia
### 3D Design Exchange Format Standards

**Goal:** Enable and facilitate intelligent Stack Design

<table>
<thead>
<tr>
<th>3D DEF WG Areas</th>
<th>Objective of a Standard</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Distribution</strong></td>
<td>Ensure that each die in the stack has access to the required power supply characteristics</td>
</tr>
<tr>
<td><strong>Thermal Management</strong></td>
<td>Ensure that no die in the stack is adversely affected by the stack level thermal hot spots or gradients</td>
</tr>
<tr>
<td><strong>PathFinding</strong></td>
<td>Facilitate input of IP constraints &amp; communication of overall stack design intent to downstream processes</td>
</tr>
<tr>
<td><strong>Stress Management</strong></td>
<td>Ensure that no die in the stack is adversely affected by the stack level stress hot spots or gradients</td>
</tr>
<tr>
<td><strong>Physical Verification</strong></td>
<td>Facilitate stack level physical DRC verification</td>
</tr>
<tr>
<td><strong>Signal Integrity</strong></td>
<td>Facilitate stack level electrical integrity</td>
</tr>
<tr>
<td><strong>DFT</strong></td>
<td>Facilitate post-stacking controllability for test application &amp; observability of test results (covered by IEEE WG)</td>
</tr>
</tbody>
</table>
Open3D TAB Target Schedule - 2013

First Batch of 3D Design Exchange Format Standards in 2013

More to follow in 2014

Silicon Integration Initiative

PDN WG
Thermal Constraints WG
Pathfinding WG

4/30/2013

Innovation Through Collaboration
Open3D TAB: Possible Future Impacts

- **OpenAccess Coalition**
  - New C++ classes or Extension Objects for Interposers, etc.

- **Low Power Coalition**
  - Extensions for LP Intent Format & LP Models

- **Design for Mfg Coalition**
  - OpenDFM Format & Parser Extensions for 2.5D/3D features

- **OpenPDK Coalition**
  - Open Process Spec. Extensions for 2.5D/3D features
Current Participants

- INVARIAN
- QUALCOMM
- SEMATECH
- GLOBALFOUNDRIES
- ATRENTA
- ANSYS
- Fraunhofer
- Texas Instruments
- SRC
- cadence
- Mentor Graphics
- IBM
- R3 Logic
- Intel
- STMicroelectronics

Silicon Integration Initiative

25th Anniversary 4/30/2013

Innovation Through Collaboration
PLEASE VISIT US @ DAC
DAC in Austin, June 3 -7, 2013

Celebrations:
DAC @ 50
Si2 @ 25
THANK YOU!