Low-Voltage Oversampling
Analog-to-Digital Conversion

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Analog-to-Digital Conversion

Quantizer model:

\[ p(e_Q) \]

Filtering \quad \text{Sampling} \quad \text{Quantization} \quad \text{Processing}

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Stanford University, 2009
Oversampling A/D Conversion

Basic concept:
Exchange resolution in time for that in amplitude through the use of oversampling, feedback and digital filtering

\[ f_S = \frac{1}{T} = \text{sampling rate} \]
\[ f_N = \frac{1}{MT} = \text{Nyquist rate} \]
\[ M = \text{oversampling ratio} \]
Oversampling

- Increasing the sampling rate ($f_s$) of an A/D converter relaxes the ANTIALIASING filter requirements.

- Increasing $f_s$ also reduces the in-band quantization noise ($N_B$); but only gain 3dB in resolution per octave increase.
**Oversampling + Feedback**

- Can combine **feedback** with **oversampling** to improve the resolution gained by oversampling.

- Feedback can be used for PREDICTION ($\Delta$ modulation) or NOISE SHAPING ($\Sigma\Delta$ modulation).

- Idea of using oversampling and feedback for analog-to-digital conversion first appeared as **delta modulation**
  

- Noise shaping (**sigma-delta**, or **delta-sigma**) modulators are more robust and easier to implement than predictive modulators.
Delta Modulation

- Quantizes the difference between \( x \) and \( q \)
- \( q \) is generated by accumulating the quantized differences
- Typically use a 1-bit quantizer with a small step size; step size can be adapted to accommodate “slope overload” (signal changing too fast)
- Fundamental problem is the accumulation of D/A mismatch error in the demodulator
Noise Shaping Modulators

- Idea of using oversampling and feedback to shape the spectrum of quantization noise first appeared in an **error feedback** oversampling modulator
  
Error Feedback $\Leftrightarrow \Sigma \Delta$ Modulation

- Move the delay to the forward path

\[
x_n \rightarrow \text{DELAY} \rightarrow y_n
\]

- Separate feedback from input and output of quantizer

\[
x_n \rightarrow \text{DELAY} \rightarrow y_n
\]
Sigma-Delta (or Delta-Sigma) Modulation *

\[ Y(z) = z^{-1}X(z) + (1 - z^{-1})E_Q(z) \]

\[ N_E(f) = \left[ 2 \sin\left( \pi f / f_S \right) \right]^2 N_Q(f) \]

ΣΔ Modulator Response
Noise Shaping

First-Order Noise Shaping

Frequency

Ideal Digital Lowpass Filter

First-Order Noise Shaping

\[ f_B \quad f_N \quad \frac{f_S}{2} \]
If it is assumed that the spectrum of the quantization error is white (which is not actually the case) and if $S_Q$ denotes the quantization error power ($S_Q = \Delta^2/12$), then

$$N_Q(f) = \frac{S_Q}{f_S} = \frac{(\Delta^2 / 12)}{f_S}$$

and the baseband quantization noise power in the output is

$$S_B = \int_{-f_B}^{f_B} N_Q(f) df = \frac{S_Q}{f_S} \int_{-f_B}^{f_B} \left[ 2 \sin(\pi f T) \right]^2 df$$

If $f << f_S = 1/T$, then

$$\sin(\pi f T) \equiv \pi f T$$

and

$$S_B \equiv \frac{\pi^2}{3} \left( \frac{1}{M} \right)^3 S_Q$$

where $M = \frac{f_S}{2f_B}$.
Higher-Order Noise-Shaping Modulators

The order of the noise shaping can be increased using either

- **Single quantizer modulators**
  - Multi-loop noise differencing
  - Single loop with multi-order filtering

or

- **Cascaded (multistage) modulators**
**Single-Quantizer ΣΔ Modulator**

\[ Y(z) = H_X(z)X(z) + H_E(z)E(z) \]

*where*

\[ H_X(z) = \frac{A(z)}{1 + A(z)F(z)} \]
\[ H_E(z) = \frac{1}{1 + A(z)F(z)} \]

*and*

\[ A(z) = \frac{H_X(z)}{H_E(z)} \]
\[ F(z) = \frac{1 - H_E(z)}{H_X(z)} \]
Noise Differencing Modulators

- \( Y(z) = z^{-1}X(z) + (1 - z^{-1})^L E(z) \)
- Can implement with a single quantizer and L nested loops
- Limit cycle instability for \( L > 2 \)
- For \( L = 2 \)

\[
A(z) = \frac{z^{-1}}{(1 - z^{-1})^2} \quad \text{and} \quad F(z) = 2 - z^{-1}
\]
Noise-Differencing $\Sigma\Delta$ Modulators

\[ S_B \approx \frac{\pi^{2L}}{(2L + 1)} \left( \frac{1}{M} \right)^{2L+1} S_Q \]

![Diagram showing noise shaping for different values of L: L=1, L=2, L=3. The diagram includes a low-pass filter (LP Filter) and frequency axes labeled $f_B$, $f_N$, and $f_{S/2}$.]
$$\Sigma\Delta$$ Modulator Dynamic Range

![Graph showing the relationship between oversampling ratio and dynamic range for different levels of noise shaping (L=1, L=2, L=3).](image)
2nd-Order Modulator Implementation

\[ A(z) \]

\[ F(z) \]

Unity Transfer Function
2nd-Order $\Sigma\Delta$ Modulator
2nd-Order $\Sigma\Delta$ Modulator

\[
\begin{align*}
X & \rightarrow \Sigma \rightarrow \Sigma \rightarrow z^{-1} \rightarrow \Sigma \rightarrow \Sigma \rightarrow z^{-1} \rightarrow \Sigma \rightarrow Y \\
\downarrow & \\
X & \rightarrow \Sigma \rightarrow z^{-1} \rightarrow \Sigma \rightarrow 2 \rightarrow \Sigma \rightarrow z^{-1} \rightarrow \Sigma \rightarrow Y
\end{align*}
\]
2nd-Order Noise-Differencing $\Sigma \Delta$ Modulator *

(with 1-bit quantization)

Quantization Noise Spectra of $\Sigma\Delta$ Modulators

$x(kT) = 0$ (midrange input; full scale $= \pm \Delta/2$)

$y(kT)$:

$\Rightarrow$ No low-frequency component

$x(kT) = (0.001)\Delta/2$

$y(kT)$:

$\Rightarrow$ Frequency component in baseband
Quantization Noise Spectra (M = 256)

First-Order $\Sigma\Delta$ Modulator

Second-Order $\Sigma\Delta$ Modulator

DC Input Level ($\Delta$) vs. Maximum Peak (dB)
Composite Spectra for Several DC Inputs
“Whitening” the Error Spectrum

- Cascaded $\Sigma \Delta$ modulation
- Multi-bit quantization
- Dither
Cascaded $\Sigma\Delta$ Modulation
Cascaded Noise-Shaping Modulator

Matches noise shaping of quantization error in first-stage
Maximum Improvement in Dynamic Range

Independent of OSR

Simulation
Closed form equation

Coefficient Mismatch (%) vs. Dynamic Range Improvement (dB)
Third-Order (2-1) Cascaded Modulator

\[ Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 E_1(z) \]

\[ Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z) \]

\[ Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})^2 Y_2(z) = z^{-3}X(z) + (1 - z^{-1})^3 E_2(z) \]
2-1 Cascaded $\Sigma \Delta$ Modulator
Matching Error in 2-1 Cascade

![Graph showing the relationship between Matching Error and Loss in Dynamic Range (dB).]

- Calculated
- Simulated

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Spectrum of 2-1 Cascade w/ Mismatch
Spectrum of 1-1-1 Cascade w/ Mismatch

Spectral Power (dB)

Frequency (kHz)
Tone Cancellation in 2-1 Cascade

![Graph showing spectral power vs. frequency for Second-Order and 2-1 Cascade systems.](image)

- Spectral Power (dB) vs. Frequency (kHz)

- Dotted line: Second-Order
- Solid line: 2-1 Cascade
Advantages of 2-1 Cascade

- Low sensitivity to precision of analog circuits
- Suppression of spurious noise tones resulting from correlation of quantization noise with input
- Design flexibility
- No potential instability
Implementation of Low-Voltage, Low-Power CMOS $\Sigma\Delta$ Modulators
Analog Integration in CMOS

- Continuous Time (tune $g_m$ or MOS-R)
  - $g_m$-C
  - MOSFET-C

- Sampled Data
  - Switched current
  - Switched capacitor
Analog Integration in CMOS

- Continuous-time ($g_m$-C or MOSFET)
  - Tune $g_m$ or MOS resistor
  - Performance limited by timing jitter, waveform asymmetry and integrator linearity

- Switched-current
  - Limitations:
    - current sources must be cascoded to increase output resistance $\Rightarrow$ high supply voltage
    - large $V_{GS} - V_T$ needed to reduce sensitivity to $V_T$ mismatch $\Rightarrow$ high power dissipation
    - sensitive to switch parasitics and charge injection
    - noise introduced into “compressed” signal

$\Rightarrow$ Switched-capacitor approach preferable for obtaining high resolution at low supply voltage and low power dissipation
Low-Power $\Sigma\Delta$ Modulator Design

- **High-resolution** converters should be limited by **thermal noise**
  - $kT/C$ noise in switched-capacitor circuits
- First stage limits performance and therefore dissipates a large fraction of power
- Minimize power by minimizing capacitor size in switched-C implementations
Example of 2nd-Order Modulator for Digital Audio

S1, S5: $\Phi_1_{\text{delayed}}$, CMOS
S2, S6: $\Phi_2_{\text{delayed}}$, CMOS
S3, S7: $\Phi_1$, NMOS
S4, S8: $\Phi_2$, NMOS
Sub-1V $\Sigma\Delta$ Modulation *

- **Motivation**
  - Driven by scaling of technology and desire to reduce power dissipation in embedded applications
  - Headroom constraints become increasingly severe
  - Look for progress in both architecture and circuits

- **Target performance objectives**
  - 0.7-V supply
  - Digital audio applications (25-kHz signal bandwidth)
  - 95-dB dynamic range
  - Minimum power dissipation (< 1.5 mW)

* Hyunsik Park
Conventional First-Order $\Sigma\Delta$ Modulator

- Integrator swings depend on input
- Large input $\Rightarrow$ nonlinear operation of integrator
Input Feedforward $\Sigma \Delta$ Modulator

- Integrator swings independent of input $\Rightarrow$ attractive at low $V_{DD}$
- Analog summation and timing overhead issues
- Approach can be extended to higher-order modulators
Second-Order Input Feedforward $\Sigma\Delta$ Modulator *

\[
U_1 = -(1 - z^{-1})^2 E \quad |U_1| \leq 2 \text{ LSB}
\]
\[
V_1 = -z^{-1}(1 - z^{-1}) E \quad |V_1| \leq \text{ LSB}
\]
\[
V_2 = -z^{-2} E \quad |V_2| \leq 0.5 \text{ LSB}
\]
\[
W_1 = X + z^{-1}(z^{-1} - 2)E
\]

\[
Y = X + (1 - z^{-1})^2 E
\]

Input feedforward removes input signal component in loop
- reduces integrator output swing
- relaxes demands on analog circuitry

But, these advantages are accompanied by
- need for analog summation at quantizer input
- timing overhead issues

* J. Silva, Elec Letters, June 2001
Oversampling w/ Multi-Bit Quantization

- Multi-bit quantization
  - reduced voltage swings within the feedback loop
  - increased dynamic range

- Potential problems
  - increased quantizer power dissipation
  - need to linearize the quantizer DAC output
Tracking Multi-bit Quantization * (4-Bit Example)

- Provides multi-bit quantization w/ fewer comparators
- Concerns
  - stability
  - increased complexity of comparator design
  - sensitivity to comparator offset mismatch

* L. Dorrer, 2005 ISSCC
Single Comparator Tracking Quantizer

- No comparator offset mismatch problem
- Smaller area and reduced integrator loading
- But timing constraints are difficult when combined with input feedforward
Delayed Input Feedforward $\Sigma\Delta$ Modulator

\[(1-z^{-1})^{L+1} \cdot X - (1-z^{-1})^L \cdot E_Q\]

\[Y = \frac{z^{-1} + H(z)}{1 + H(z)} \cdot X + \frac{1}{1 + H(z)} \cdot E_Q\]

if \[\frac{1}{1 + H(z)} = (1-z^{-1})^L\]

\[Y = (1-(1-z^{-1})^{L+1}) \cdot X + (1-z^{-1})^L \cdot E_Q\]
Proposed Low-Voltage ∑Δ Modulator

Delayed Input Feedforward

Single Comparator Tracking Multi-bit Quantizer (18 Levels)

\[
\frac{0.9 \cdot z^{-1}}{1 - z^{-1}} + \frac{z^{-1}}{1 - z^{-1}}
\]

Reference Update

Decision Logic & Counter

Fast

DWA

Slow

MUX

MUX

Y
Signal Swing Comparison

2) Conventional 2nd-order distributed f/b w/ 4-bit quantization (no integrator gain scaling)

3) Yao, 2004 ISSCC

4) Ahn, 2005 ISSCC

5) Rabii, JSSC, June 1997
Modulator Implementation

*Actual implementation is fully differential*
First Integrator Op Amp

- Incomplete, but linear, settling in op amp ⇒ low power

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>48.8 dB</td>
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<tr>
<td>Power</td>
<td>350 µW</td>
</tr>
<tr>
<td>$BW_u$</td>
<td>18.9 MHz @ 18pF loading</td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>0V (Input), 0.35V (Output)</td>
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</tbody>
</table>
Chopper Stabilization Circuit

Switch Symbols
- NMOS switch
- NMOS switch with local gate bootstrapping

Timing Diagram
- $\Phi_1$ (Sampling)
- $\Phi_2$ (Integration)
- $S_A, S_A^d$
- $S_B, S_B^d$
Analog Summation and Quantizer
Comparator Preamps

When cascaded, $S_1$, $S_2$: Bootstrapped NMOS Switch

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tr>
<td>DC Gain</td>
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<tr>
<td>$BW_{open-loop~3dB}$</td>
<td>174 MHz</td>
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<tr>
<td>Power</td>
<td>149 μW</td>
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<tr>
<td>$BW_{closed-loop~unity}$</td>
<td>140 MHz</td>
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<tr>
<td>$3-\sigma \Delta V_{os}$</td>
<td>19 mV</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>58 Degree</td>
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</table>
Comparator Latch

\[ V_{DD} = 0.7V \]

<table>
<thead>
<tr>
<th>Average Power</th>
<th>(~14 , \mu W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{\text{regen}}) @ 5 mV_{pp} input</td>
<td>(~2.1 , \text{nsec})</td>
</tr>
<tr>
<td>3-(\sigma) (V_{OS})</td>
<td>23 mV</td>
</tr>
</tbody>
</table>

*S. Limotyrakis, ISSCC 2004*
Low-Voltage Switch: Local Bootstrapping *

- Used to process dynamic signals with high precision

* M. Dessouky, JSSC, March 2001
Low-Voltage Switch: Local Boosting

- Used to process DC signals near ground
Chip Photograph
Measured SNR and SNDR
Measured Output Spectrum

-5 dB, 1-kHz input sinusoid
### Performance Summary

<table>
<thead>
<tr>
<th>Metric</th>
<th>Value</th>
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<tbody>
<tr>
<td>Supply Voltage</td>
<td>0.7 V</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>5 MHz</td>
</tr>
<tr>
<td>References</td>
<td>0 V, 0.7 V</td>
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<tr>
<td>Signal Bandwidth</td>
<td>25 kHz</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>100 dB</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>100 dB</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>95 dB</td>
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<tr>
<td>Power: Analog</td>
<td>680 μW</td>
</tr>
<tr>
<td>Digital</td>
<td>190 μW</td>
</tr>
<tr>
<td>Area (excluding decoupling caps, pads &amp; output drivers)</td>
<td>2.16 mm²</td>
</tr>
<tr>
<td>Technology</td>
<td>0.18-μm CMOS</td>
</tr>
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Summary

- Oversampling offers a means of exploiting the design and test methodologies of digital circuit design, as well as the scaling of CMOS technology, to realize robust data conversion interfaces.

- Even at supply voltages as low as 0.7V, it is possible to achieve digital audio performance using switched-capacitor circuits implemented in conventional CMOS technology.

- Related research at Stanford includes low-voltage cascaded $\Sigma\Delta$ modulation for MHz bandwidth A/D conversion.
  - Target objectives: 1V (or lower) supply, ≥ 2-MHz bandwidth, 90-dB dynamic range, minimum power dissipation.