IEEE SCV Circuits and Systems Society

Two-Day Short Course

Emerging Frequency Synthesis Techniques for the Current and Future Advanced CMOS Technologies

August 14th-15th (Saturday/Sunday), 2010, 9:00am-6:00 pm
QualComm Santa Clara, Bldg. B Cafeteria
3165 Kifer Road, Santa Clara, CA

Fees:

- $40/IEEE member ($50 non-member) for advance registration (priori to 8/6/2010).
- Add $20/person for at door registration.
- Free for Student (ID required) and unemployed (Need to send $15 check for advance registration. The check will be returned at the on-site registration).
- Registration fee includes donuts and coffee for breakfast and lunch box for both days.
- Contact: TLoan at tln.sv@ieee.org or 408 465-0311 (cell).
- Send Check to*: Dr. Mark S. Hooper*
  IEEE SCV CAS Secretary
  211 Stockbridge Ave.
  Atherton, CA 94027
- Make check payable to "IEEE SCV CAS".

Description of the event

The task of clock-generation becomes increasingly difficult as we move into the nanometer-scale CMOS technologies. The single most dominant reason behind these difficultness is that these advanced CMOS technologies are designed mainly to handle digital signals. They are not analog friendly. The traditional electronic circuitry is naturally destined to handle its internal signal's voltage/current *level*, not the *timing*. Within the electronic circuitry, the timing information is only indirectly implied by its signal's crossing of certain voltage/current threshold levels. Therefore, traditionally, the task of clock-generation (where timing is the primary design variable) is mainly dealt with by analog-intensive circuitry since the traditional analog circuitry can handle much more voltage/current levels than its digital counterpart can. When chip design moves into the regime of advanced CMOS nodes where two-level digital signal is the main design entity, innovative timing approaches have to be created to meet this new challenge: using best of the digital plus minimum of analog.

On another front, modern designs suffer from excessive on-chip component-count, and are extremely complex in terms of functionality. To support this large number of sequential elements and sophisticated timing requirement, the on-chip clock-generation-circuitry has to be efficient both in producing frequencies and in consuming resources (area, power, etc). The clock circuitry designer is constantly under tremendous pressure of creating better designs at lower cost.

The task of clock-generation is at the central focus point of modern VLSI design. To find better solutions for future, researchers and engineers around the world are relentlessly exploring various methods. Among them, two approaches have emerged with great potential: *Time-Average-Frequency based Flying-Adder frequency synthesis technology* and *All Digital PLL* (*ADPLL*, see book in SC#3, page 4). Both of them are born from the battleground of designing real commercial products. In this short course, these two emerging technologies will be introduced in great detail.

Agenda

SC#1: 8/14/10 9 am –12 am, Paul Sotiriadis.

- Overview of Digital-Intensive Frequency Synthesis Architectures: Current Trends and Future Directions.
- Mathematical theory of Time-Average frequency generation based on the Flying-Adder frequency synthesizer and similar digital architectures.

SC#2: 8/14/10 1 pm – 6 pm, Liming Xiu.

- Time-Average-Frequency Based Flying-Adder Frequency Synthesis Technology: the circuit implementation and the system application.

SC#3: 8/15/10 9 pm – 6 pm, R. Bogdan Staszewski.

- All-Digital Frequency Synthesizer in Deep-Submicron CMOS.

Courses Description:

SC#1: Paul Sotiriadis

Course Content

This section presents the current trends and future directions of the two classes of digital-intensive frequency synthesis architectures: the ones using an internal oscillator and the ones that don't. Comparative advantages and disadvantages of the two classes are discussed. The concept of Time-Average-Frequency and its generation is introduced and formulated mathematically. The Flying-Adder and similar digital frequency synthesizer architectures are considered and their Timing and Spectral properties are discussed in detail along with dithering and spurs-suppression techniques. Guidelines are given to help the designer choose the synthesizer's parameters based on the applications' requirements. Finally, open problems are discussed related to extending the application area of Time-Average-Frequency generators.

Course Outline (Tentative)

Part I: Digital-Intensive Frequency Synthesizers: Current Trends and Future Direction.
Part II: Rigorous formulation of the Time-Average-Frequency concept.
Part III: Pulse DDS: Timing and Spectral properties
Part IV: The Flying-Adder frequency synthesizer: Timing and Spectral properties
Part V: Spurs suppression techniques
Part VI: Open problems

Literature and Study Materials

Handouts
IEEE Publications

Instructor's Biography

Paul P. Sotiriadis (S'99, M'02) received the Ph.D. degree in EECS from the Massachusetts Institute of Technology in 2002 under the supervision of Prof. Anantha Chandrakasan, and the MSEE from Stanford University in 1996. In 2002 he joined Johns Hopkins University as assistant professor of ECE. In 2007 he joined Apex/Eclipse INC as the Chief Technology Officer and shortly after he started Sotekco Electronics LLC, an electronics research company in Maryland, USA. He is interested in the design, optimization, and mathematical modeling of analog, mixed-signal RF and microwave

circuits with special emphasis in advanced frequency synthesis and deep-sub-micron technologies. He has led several projects in these fields funded by US organizations and has collaborations with industry and National labs. He has authored and co-authored more than seventy technical papers in IEEE journals and conferences, most of them as the leading or single author. He has served as an associate editor of the IEEE Transactions on Circuits and Systems II and is a member of several technical and conference committees.

SC#2: Liming Xiu

Course Content

In this course, Time-Average-Frequency concept is introduced first. Then, Flying-Adder architecture will be described. The circuit implementation detail is explained next. Comparison with other techniques is also included. Following that, the Digital-to-Frequency Converter (DFC) is presented. The DFC-based information processing approach is discussed. Further, several systems extracted from real commercial products are used as examples to demonstrate the power of this new frequency generation technique.

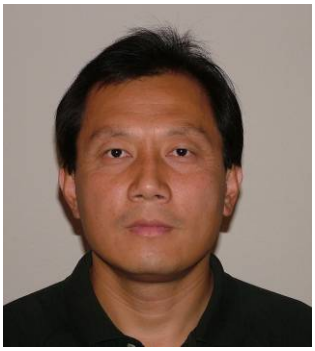
The Flying-Adder-related-techniques is circuit-level enabler for system-level innovations. This is a new field with great research potential and commercial value. There are still many unsolved issues related to the theoretical understanding of the Time-Average-Frequency, especially in frequency domain. There are also many unexplored opportunities of applying these techniques in new commercial applications. Therefore, in the last section of this tutorial, unsolved problems and future directions will be discussed. The presenter will share many new ideas, which have not been carried out due to either behind-schedule or beyond-his-capability, with the audience and ask for help. These topics are very suitable for PhD research.

Course Outline

Part I: The Concept of Time-Average-Frequency (TAF)
Part II: The implementation: Flying-Adder frequency synthesis technology
Part III: The Digital-to-Frequency Converter (DFC)
Part IV: The DFC based information processing approach
Part V: Commercial examples: a circuit-level enabler for system-level innovations
Part VI: The unsolved problems and the opportunities for future

Instructor's Biography

IEEE CAS VP for Region 1-7.
Chief Clock Architect, Novatek (novatek.com.tw).
Senior Member of Technical Staff (SMTS), Texas Instruments Inc. 1995-2009.



Liming Xiu is the inventor of Flying-Adder frequency synthesis architecture which has been used in many commercial products with revenue of over 500-millions US dollar. During his professional career, he has published many journal papers on Flying-Adder related topics. He holds sixteen granted and pending patents. He is also an industry expert on VLSI SoC integration with battle-proven integration experience on several very large chips in advanced CMOS nodes. In this area, he has one book published: "VLSI Circuit Design Methodology Demystified". Both TI CEO (Richard Templeton) and CTO (Hans Stork) have written forewords for this book. Liming Xiu has the experience and skill of a practical engineer. Moreover, he also possesses the vision and capability of a frontline researcher with energetic passion for innovation. His career goal is to spread this groundbreaking Flying-Adder/Time-Average-Frequency/Digital-to-Frequency-Converter technology within the industry, to serve the mission of creating cheaper, better, more efficient electronic products.

Literature and Study Materials

Handouts
IEEE Publications

SC#3: R. Bogdan Staszewski

Course Content

The past several years have successfully brought all-digital techniques to radio frequency (RF) frequency synthesizers and transmitters. In addition, digital assistance is applied to RF circuits to improve performance and power consumption. This course will introduce basic concepts of the digital RF frequency synthesis approach and walk though the major building blocks that comprise the new RF transceiver architecture:

- All-digital phase-locked loop (ADPLL) comprising: digitally-controlled oscillator (DCO), time-to-digital converter (TDC), and digital loop filter.
- All-digital transmitter featuring ADPLL with wideband modulation capability, and comprising digitally-controlled power amplifier (DPA)

Literature and Study Materials

- Book: R. B. Staszewski and P. T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS*, New Jersey: John Wiley & Sons, Inc., Sept. 2006. ISBN: 978-0471772552.
- Selected IEEE publications

Course Outline

A total of seven intensive lecture hours:

1. Introduction to the topics of digital RF and digital assistance of RF.
2. Digitally-controlled oscillator (DCO); phase noise modeling and simulation
3. DCO interface: sigma-delta modulation, dynamic element matching, DCO gain normalization
4. Principles of phase-domain frequency synthesis: all-digital PLL (ADPLL)
5. Time-to-digital converter (TDC) and metastability
6. ADPLL closed-loop behavior
7. Direct frequency modulation of ADPLL

Instructor's Biography

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R. Bogdan Staszewski received BSEE (summa cum laude), MSEE and PhD from University of Texas at Dallas in 1991, 1992 and 2002, respectively. From 1991 to 1995 he was with Alcatel in Richardson, TX, USA. He joined Texas Instruments in Dallas, TX, USA in 1995. In 1999 he co-started a Digital RF Processor (DRPTM) group with a mission to invent new digitally-intensive approaches to traditional RF functions. Dr. Staszewski was appointed a CTO of the DRP group between 2007 and 2009. Since July 2009 he is Associate Professor at Delft University of Technology in the Netherlands. He has co-authored one book, two book chapters, 110 journal and conference publications, and holds 60 issued 40 pending US patents. His research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters and receivers. He is an IEEE Fellow.