Advanced EDA Tools for Multi-Radio High-Frequency Accurate IC Design

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INTRODUCTION

TRENDS

- **Multiband**
  - Number of different radios / wireless device is growing.

- **Design Cycles**
  - Time allowed for design is shrinking.

- **Size**
  - Amount of area for any given function is shrinking.

- **Clock Speed**
  - IC operating speed is increasing.

- **Application Frequency**
  - New applications are increasing operating frequency.

- **Product Lifecycles**
  - Lifetime of any given product is shrinking.

- **Internet of Things**
  - Number, standards and types of devices growing rapidly.
INTRODUCTION

RF DESIGN CHALLENGES

• Iterations
  › Generally the longest time, not to mention cost, for a single iteration is the prototype fabrication time.
  › Reduced number of design iterations is necessary to meet time-to-market expectations.
  › Improved simulation accuracy is required in order to reduce the number of iterations, yet the number of design passes to meet the specification has not changed substantially over the last 20 years.

• Tools
  › Electronic Design Automation (EDA) has roots in two basic approaches:
    – Circuit simulators
    – EM Field solvers
  › To overcome the limitations of both, EDA tools have incorporated the ability to paste in blocks of simulation results to permit “co-simulation” of circuit and EM results.
  › This approach is limited in its ability to accurately simulate circuit response and hence does not reduce the number of design cycles.
INTRODUCTION

RF DESIGN CHALLENGES

Wire bond

Passives

Transistor
EDA Evolution

EVOLUTION / ACCURACY

Circuit simulation

HYBRID Circuit + Blocks

EM-Supreme®
## EM SIMULATOR COMPARISON

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<thead>
<tr>
<th>Company</th>
<th>PedaSoft</th>
<th>Sonnet</th>
<th>CST</th>
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Why Fully Integrated Solution?

Fully Integrated Solution features:

- Layout can be dissected to look at:
  - Coupling
  - Isolation
  - Interference
- Transient Analysis of Subcircuits
- Tx / Rx Multitone Analysis
- Load Pull / Source Pull
- Gain & Harmonics
- Radiation
- Software can be customized to meet specific customer requirements.
EM-SUPREME® OVERVIEW

EM-SUPREME®

• Finite Difference Time Domain (FDTD) model that uses no approximations.
• The tool models electromagnetic fields as they pass through the active and passive components to predict real circuit performance as it physically happens.
• IC, passives, substrate and package are all included in the model.
• Compatible with existing design tools to minimize learning curve.
• Two modes of operation:
  › Stand alone – Provides all necessary tools to completely model a given component or module.
  › Optimization – Adds on functionaility and its side by side to existing tools to improve prediction of the actual circuit performance.
CONTENTS

✓ Introduction
✓ EM-Supreme® Overview

➢ Design Flow
  Examples
  Demonstration
  Engagement
  Summary & Conclusion
PORTABILITY

- Circuit Simulation (i.e. ADS)
- Circuit + Layout Simulation (i.e. ADS + Momentum)
- Circuit + Layout + Package Simulation (i.e. ADS + Momentum)
- Circuit + Layout + Package + PCB Simulation (i.e. ADS + Momentum)

DXF / GDS

EM-Supreme®
Total / Active + Passive / Simultaneous System Evaluation
DESIGN FLOW

OPTIMIZATION MODE

Design Specification
Schematic Capture
Simulation
Layout
Dsgn Rule Check (DRC)
Parameter Extraction
Lay vs Sch Check (LVS)
Final Simulation
Tape Out

PedaSoft Solution

Layout Transfer Verification
Passives
Actives + Passives

DXF GDS

Active Model Insertion

EM-Core® Simulation
Parameter Extraction

EM-Supreme® Simulation
Parameter Extraction

Schematic Conversion

Tape Out

Passives
Actives + Passives

EM-Core® Simulation
Parameter Extraction

EM-Supreme® Simulation
Parameter Extraction

Schematic Conversion

Tape Out
ACTIVE MODELS

- PedaSoft’s EM-Supreme® can accept any model:
  - Spice, Curtice, Angelov, Stats-Pucel, ...
  - Foundry PDK, TOM, Customer proprietary, ...

- PedaSoft customized
  - For optimal results PedaSoft will take any of the above models and work with the manufacturer / foundry to optimize the model for use in EM-Supreme®.
Many potential sources of error

- New Dimensions results when EM Simulating the whole structure "i.e. feedback network and vias."
- The feedback line could EM-couple with the substrate, packaging layers, and neighborhood components
- The transistor along with feedback network exist on the top layer of a multilayer substrate with metallization underneath, adding possibilities of coupling that designer needs to account for.
PA DESIGN

2 – 5 GHz flat gain target

Transistor + VIAs + Feedback Network + PCB
PA DESIGN (cont.)

A1 = 0.2595
A1 = 0.3595
A1 = 0.4595

S11 (dB)

S21 (dB)

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A3 = -0.0305
Alpha = 1.000
Ri = 1.000
Rs = 0.700
Rg = 0.500
Rd = 0.500
VGG = -0.810
VDD = 18.960
Signal Simulations = Large
Temperature = 300.000
Power Sweep (dBm) = 10.000
Power Sweep Min (dBm) = 0.000
Power Sweep Max (dBm) = 30.000
Input Frequency (GHz) = 6.000
PA DESIGN (cont.)

![Graphs showing PA performance metrics including S11 and S21 in dB vs. Frequency (GHz) at different Pin levels.]

- S11 (dB) vs. Frequency (GHz) showing a deep null at certain frequencies for the second harmonic.
- S21 (dB) vs. Frequency (GHz) showing a high gain response with decreasing gain as frequency increases.

These graphs illustrate the key performance metrics for a power amplifier (PA) design, showcasing its efficiency and bandwidth capabilities.
PA DESIGN (cont.)

• Comparison of same circuit using co-simulation

![S21 (dB) vs. Frequency (GHz)](image1)

![S11 (dB) vs. Frequency (GHz)](image2)
EXAMPLES

PIN SWITCH

Contact Resistance (Ohms) | 0.500
Intrinsic Area (cm²)     | 5.260e-006
Int. Area Width (cm)     | 2.000e-004
Technology               | GaAs
Bias current (A)         | 3.000e-002
Doping_N (cm⁻³)          | 1.000e+019
Doping_P (cm⁻³)          | 1.000e+018
Reverse Voltage (V)      | 10.000
Power Sweep (dbm)        | 1.000
Power Sweep Min (dbm)    | 10.000
Power Sweep Max (dbm)    | 20.000
Input Frequency (GHz)    | 40.000
FoundryModel (On-State)  |
FoundryModel (Off-State)  |

Name                    | PinDiode1
Startx                  | 300.000
Starty                  | 100.000
Startz                  | 150.000
Endx                    | 300.000
Endy                    | 166.867
Endz                    | 150.000
From Metal              | Bridge1
To Metal                | Square10
State                   | On
Signal Simulations      | Small
Number of Contacts      | 1.000
Saturation Current (A)  | 1.000e-014
Turn-on Voltage (V)     | 0.700
PIN SWITCH (cont.)

- $s_{21}$ (dB)
  - $R_r = 0.5$
  - $R_r = 1$
  - $R_r = 2$

- $s_{11}$ (dB)
  - $I_s = 1e^{-14}$
  - $I_s = 2e^{-14}$
  - $I_s = 3e^{-14}$

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EXAMPLES

PIN SWITCH

• Diode only
PIN SWITCH (cont.)

• Add VIAs
Integrated Switch/Antenna Module

Measurements versus EM-Supreme
Measurement versus EM-Supreme

Radiated Emissions

E-Field

H-Field

Two EVB Xmission Line Lengths
SUMMARY & CONCLUSION

- EM-Supreme includes electromagnetics to model field distributed-effects, coupling, radiation, as well as parasitic effects at RF and millimeter-wave bands; for active, passive, and complete RF modules.

- Technology supported includes, but not limited to, PHEMTS, Silicon Germanium, Gallium Arsenide, Aluminium Gallium Arsenide, Indium Gallium Phosphide HBT’s and PIN diodes. With the method, RF designer can model CMOS as well as Gallium Arsenide and Gallium Nitride FETs.

- EM-Supreme **eliminates** excessive design cycles (typically 3 to 4) and/or inefficient designs which would translate into high costs and ultimately lost time-to-market opportunities.
EM-Supreme is the first EM simulator for the whole chip “transistors plus passives” to including all parasitic effects, radiation coupling and inference in a single software tool.

The tool is fully customized. The tool comes as a stripped or customized version based on special foundry or active models “i.e. cost effective and flexible”

Easy to Use “just import the layout in DXF and then insert active components”

We have a very well established team "programmers, GUI's, RF engineers, and packaging designers”

The current version is very stable version that has been used by dozens of RF engineering teams

Windows compatible “can run efficiently on any windows operating system including windows 7.0”
Thanks You

More info. can be found at

www.pedasoft.com

or email me at

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