Continuous-time \( \Delta \Sigma \) Modulators with Improved Linearity and Reduced Clock Jitter Sensitivity using the SCRZ DAC

Shanthi Pavan
Indian Institute of Technology, Madras
Chennai 600 036
- Work of my M.S students
  - Timir Nandi, now at TI, India
  - Karthikeya Boominathan
- Part of this presented at
  - CICC 2012
Outline

- Introduction
- Limitations of conventional DAC pulses
- Switched-C Return-to-Zero Principle
- Modulator Architecture
- Circuit Design
- Measurement Results
- Conclusion
Motivation

- Continuous-time DSMs
  - Resistive input impedance
  - Relaxed opamp gain requirements
- Most high performance CTDSMs
  - Multibit loops
- Focus of this research
  - Can we do better with single-bit loops?
- Case study
  - 14 bit ENOB, 2 MHz Bandwidth, 0.18μm CMOS
Multibit versus Single-bit Modulators
## Design Targets

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic Range</td>
<td>86dB (14 ENOB)</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>2 MHz</td>
</tr>
<tr>
<td>Order</td>
<td>4</td>
</tr>
<tr>
<td>Quantizer</td>
<td>1 bit</td>
</tr>
<tr>
<td>Out of Band Gain</td>
<td>4 bit</td>
</tr>
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<td></td>
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<tr>
<td><strong>Out of Band Gain</strong></td>
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<tr>
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</tr>
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<tr>
<td><strong>OSR Needed</strong></td>
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<tr>
<td></td>
<td><strong>80 MHz</strong></td>
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</table>
ADC : 1 bit versus 4 bit

- 4 bit ADC
  - 15x more comparators @ 1/3\textsuperscript{rd} speed
  - 5x more ADC power, 15x more area
  - 15x loop filter & clock path loading
DAC : 1 bit versus 4 bit

- 4 bit DAC
  - Needs Dynamic Element Matching
  - DEM adds excess delay & power
  - Not very effective @ low OSR
DAC: 1 bit versus 4 bit

A single bit quantizer consumes lesser power though it operates at 3x the speed

Calibration

- Complex logic
Modeling Clock Jitter

\[
\begin{align*}
V_{\text{in}}(t) &\quad \sum \quad H(s) \quad \text{ADC} \quad V_{\text{out}}[n] \\
V_{\text{dac}}(t) &\quad + \quad \text{DAC} \\
V_x &\quad \text{DAC} \quad \equiv \quad \text{DAC} \quad e_1(t) \\
\text{Clock} &\quad \text{Clock}
\end{align*}
\]
Clock Jitter Comparison

A 4-bit modulator can tolerate 15 times more RMS white jitter compared to a single bit design.

\[ e[n] \approx (V_{out}[n] - V_{out}[n - 1]) \frac{\Delta t_n}{T_s} \]
Loop Filter Linearity

Higher demands on loop filter linearity

$V_{in}(t)$

$V_{dac}(t)$

$H(s)$

ADC

DAC

$V_{out}[n]$
Choice of Quantizer

- Single bit quantizer
  - Lower power ADC
  - No DEM needed
  - Sensitive to clock jitter
  - Loop filter needs to be extremely linear

Try to fix this
DAC Pulse Shapes: NRZ

Inherently nonlinear (rise-fall asymmetry)
DAC Pulse Shapes: NRZ

\[ \frac{T_{rise} - T_{fall}}{T_s} = 1\% \]

\[ HD_2 \approx 55 \text{ dB}! \]

\[ HD_2 \approx 90 \text{ dB (diff. operation)} \]
DAC Pulse Shapes : NRZ

\[ J_{RMS}^2 = 16\lambda \frac{I_o^2}{OSR} \frac{\sigma_{\Delta t}^2}{T_s^2} \]

Opamp virtual short
DAC Pulse Shapes: RZ

\[ V_{in}(t) \xrightarrow{\Sigma} H(s) \xrightarrow{\text{ADC}} V_{out}[n] \]

\[ V_{dac}(t) \]

\[ I_{dac} \]

\[ 0 \quad t/T_s \quad 1 \]
Digression: Weak Nonlinearities in CTDSMs
RZ DAC: Linearity

- NRZ DAC: SNDR 90.7 dB
- RZ DAC: SNDR 96.2 dB

Signal Bandwidth = 2 MHz
\[ J_{RMS}^2 = 32 \frac{I_o^2}{OSR \cdot T_s^2} \sigma_{\Delta t}^2 \]

4.5 dB worse than an NRZ DAC.

- \( I_o \)
- \( V_{dd} \)
- Opamp virtual short
- Modulator output
- Jitter
- \( \phi_2 \)
- \( 2I_o \)
- Ideal
- Jittered

Graphical representation of the circuit and timing diagrams.
**Excellent** linearity

**Terrible** for jitter!
SC DAC

- Capacitors are charged to $\pm V_{ref}$ during $\Phi_1$
- They are discharged into the loopfilter during $\Phi_2$
- Charge transferred = $\pm CV_{ref}$
SC DAC

- Capacitors are charged to $\pm V_{\text{ref}}$ during $\Phi_1$
- They are discharged into the loopfilter during $\Phi_2$
- Charge transferred = $\pm CV_{\text{ref}}$

\[
\text{Peak} = I_o \frac{T_s}{T}
\]
SC DAC with Jitter

- Transfers most of the charge in a short period

\[ J_{RMS}^2 = 8 \frac{I_o^2}{OSR} \left( \frac{T_s}{\tau} \right)^2 \exp \left( - \frac{T_s}{\tau} \right) \frac{\sigma^2_{\Delta t}}{T_s^2} \]
SC DAC

- DAC output peak current is higher
- Higher demands on the linearity of the loop filter

(a) RZ DAC waveform
(b) SC DAC waveform
DAC Pulse Shapes : SC

Terrible linearity!

Excellent for jitter
Introducing the SCRZ DAC

- **RZ DAC**
  - Excellent linearity
  - High jitter sensitivity

- **SC DAC**
  - Low jitter sensitivity
  - Poor linearity

- **SCRZ DAC**
Introducing the SCRZ DAC

Opamp inputs

DAC currents

$V_{cm} + V_{ref}$

$V_{cm} - V_{ref}$

$2I_0$

$2I_0$

$V_{dd}$
SCRZ DAC operation ($\Phi_1$)
SCRZ DAC operation ($\Phi_1$)
SCRZ DAC operation ($\Phi_2$)
SCRZ DAC operation ($\Phi_2 = 0.5T_s$)

$$2I_o = CV_{ref} / (0.5T_s)$$

$$V_{xy} = 0$$

Diagram showing the operation of SCRZ DAC with the relationship $2I_o = CV_{ref} / (0.5T_s)$ and the voltage $V_{xy} = 0$. The diagram includes a circuit with nodes A, B, C, and X, and waveforms for $2V_{ref}$ and $I_{o,d}$.
SCRZ DAC operation ($\Phi_3$)
SCRZ DAC operation ($\Phi_3$)
Summary: Ideal Waveforms

- With an ideal clock
- With ideal current \( 2I_o = CV_{\text{ref}}/(0.5T_s) \)
  - \( I_{\text{dac}} \) has an RZ pulse shape
Effect of jitter

- Ideal – $\phi_2$ half clock cycle wide
- Jittered - $0.5T_s + \tau$
Effect of Jitter

\( I_{\text{dac}} \) lasts longer than \( 0.5T_s \)

\( V_{xy} < 0 \) at end of \( \phi_2 \)
Waveforms ($\Phi_3$)
Total DAC Charge

\[ Q_{dac} = C(V_{xy,initial} - V_{xy,final}) \]
Total DAC Charge

Irrespective of Jitter!

\[ A_1 - A_2 = CV_{ref} \]
Role of current source

- Shapes the capacitor discharge pulse
- Smaller peak current
- Relaxed requirement - linearity of the loop filter
Non ideality - Deviation of $2I_o$

- $2I_o(0.5T_s) = CV_{ref}$
- $I_{o,d} = 2CV_{ref}/T_s$
- Capacitors completely discharged at the end of $\Phi_2$
- $I_{dac} = 0$ during $\Phi_3$
If \(2I_o < I_{o,d}\)

- Capacitors are incompletely discharged
- The residual charge is discharged during \(\Phi_3\)
- \(I_{\text{dac}}\) is positive during \(\Phi_3\)
- Net charge supplied by the DAC remains \(\pm CV_{\text{ref}}\)
If $2I_o > I_{o,d}$

- Capacitors are over discharged
- The capacitors are charged during $\Phi_3$
- $I_{dac}$ is negative during $\Phi_3$
- Net charge supplied by the DAC remains $\pm CV_{ref}$
Tune $2I_o$

- $2I_o = I_{o,d}, \quad V_{xy} = 0$
- $V_{xy} < 0, \quad 2I_o > I_{o,d}$
Tune $2I_o$

- Comparator: sign of $V_{xy}$ at the end of $\Phi_2$
- Control $I_o$ to 6-bit accuracy
Compare: SC versus SCRZ DAC

Graphs showing

\[ \left( \frac{J}{J_{\text{RZ}}} \right)^2 \]

and

Peak-to-Average Ratio

against

\( T_s / \tau \)
Related Work : The SCSR DAC

Anderson et. al. : IEEE JSSC 2009
Related Work: The SCSR DAC
Target Modulator Specifications

- Signal Bandwidth = 2 MHz
- Sampling frequency = 256 MHz
- Quantizer range = $3.6 \ V_{pp,d}$
- Target resolution = 14 Bits
- 0.18 μm CMOS process
Noise Transfer Function

4th order NTF
OSR = 64
Maximally flat
OBG = 1.5
Peak SQNR = 100 dB
Modulator Architecture

4th Order Cascade of Integrators with Feed Forward (CIFFF)

Active-RC Integrators

Capacitive Summation
Assisted Opamp Technique

Opamp Design

(a) $V_{in}/R$

$V_{in}$

$V_{dac}$

DAC

$(+/-)I_{ref}$

Feedforward Opamp

$-g_{m1}$

$V_{x1}$

$V_{x2}$

$g_{m2}$

$-g_{mf}$

$C$

$i_1$
Two Stage Feedforward Compensation

![Circuit Diagram]

- **V_{dda}**: Power supply voltage for the circuit.
- **V_{om1}**: Output voltage of the first stage.
- **V_{op1}**: Output voltage of the second stage.
- **M_{4}**, **M_{5}**, **M_{6}**, **M_{7}**: Transistors forming the first stage of the circuit.
- **R_{CM}**: Resistance for CMFB compensation.
- **C_{CM}**: Capacitance for CMFB compensation.
- **C_{c}**: Capacitance for feedback compensation.
- **V_{ip}**: Input voltage for the circuit.
- **V_{im}**: Input voltage for the feedback compensation.
- **V_{tail}**: Voltage for tail current generation.
- **V_{op}**: Output voltage of the circuit.

- **30 \mu A**: Current through **M_{6}**.
- **230 \mu A**: Current through **M_{1}**.
- **2.4 mA**: Current through **M_{12}**.
Chip layout and test board
Test Setup

- Signal source: Agilent-33250A
- Balun: ADT1-1WT
- Test Chip
- Data
- Oscilloscope (DSO80204B)
- MATLAB
- Clock source: Centellax TG1C1A
- Computer
SN(D)R vs Input Amplitude

Dynamic range = 87.1 dB
PSD of modulator

Clock jitter
~ 1 ps rms

18 dB

SCRZ mode (SNDR 82.3 dB)
RZ mode (SNDR 64.1 dB)
Controlled jitter experiment

<table>
<thead>
<tr>
<th>FM Modulation</th>
<th>Test Board</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal Generator → Clock source</td>
<td>Modulator</td>
</tr>
</tbody>
</table>

Agilent 33250A

FM modulated sampling clock

\[ \cos \left[ 2\pi f_s t + A \cos(2\pi f_m t) \right] \]

Chosen so that RMS jitter is 50 ps

60 MHz
PSD of modulator (jittery clock)

Frequency (MHz)

PSD (dBFS)

28 dB

SCRZ mode
RZ mode
Effect of opamp assistance

- Assistant on (SNR 84.5 dB)
- Assistant off (SNR 80.0 dB)
## Performance Summary

<table>
<thead>
<tr>
<th>Signal Bandwidth / Clock Rate</th>
<th>2 MHz / 256 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Scale</td>
<td>3.6 $V_{pp,\text{diff}}$</td>
</tr>
<tr>
<td>Input Swing for peak SNR</td>
<td>-2.75 dBFS</td>
</tr>
<tr>
<td>Dynamic Range/ SNR/ SNDR</td>
<td>87.1 dB/ 84.5 dB/ 82.3 dB</td>
</tr>
<tr>
<td>Active area</td>
<td>0.38 mm$^2$</td>
</tr>
<tr>
<td>Process / Supply Voltage</td>
<td>180 nm CMOS / 1.8 V</td>
</tr>
<tr>
<td>Power (including references)</td>
<td>16.5 mW</td>
</tr>
<tr>
<td>FoM (SNR)</td>
<td>300 fJ/lvl</td>
</tr>
<tr>
<td>FoM (SNDR)</td>
<td>387 fJ/lvl</td>
</tr>
<tr>
<td>FoM (DR)</td>
<td>168 dB</td>
</tr>
</tbody>
</table>


Comparison with other works

<table>
<thead>
<tr>
<th>Reference</th>
<th>This Work</th>
<th>Anderson JSSC09</th>
<th>Veldho JSSC03</th>
<th>Gealow VLSI11</th>
<th>Kim VLSI11</th>
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<tbody>
<tr>
<td>BW (MHz)</td>
<td>2</td>
<td>1.92</td>
<td>1.23</td>
<td>1.92</td>
<td>1.95</td>
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<td>DR (dB)</td>
<td>87</td>
<td>70</td>
<td>83</td>
<td>83</td>
<td>79</td>
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<td>SNR (dB)</td>
<td>84.5</td>
<td>66.4</td>
<td>83</td>
<td>-</td>
<td>74.3</td>
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<td>SNDR (dB)</td>
<td>82.3</td>
<td>62.4</td>
<td>-</td>
<td>78</td>
<td>73.3</td>
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<td>Power (mW)</td>
<td>16.5</td>
<td>5.0</td>
<td>4.1</td>
<td>2.8</td>
<td>8.55</td>
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<td>FoM&lt;sub&gt;DR&lt;/sub&gt; (dB)</td>
<td>168</td>
<td>156</td>
<td>168</td>
<td>171</td>
<td>163</td>
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<tr>
<td>FoM&lt;sub&gt;SNR&lt;/sub&gt;(fJ/lvl)</td>
<td>300</td>
<td>768</td>
<td>145</td>
<td>-</td>
<td>517</td>
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<td>FoM&lt;sub&gt;SNDR&lt;/sub&gt;(fJ/lvl)</td>
<td>387</td>
<td>1218</td>
<td>-</td>
<td>110</td>
<td>580</td>
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<td>Tech. (nm)</td>
<td>180</td>
<td>90</td>
<td>180</td>
<td>40</td>
<td>65</td>
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<td>Supply (V)</td>
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<td>1.2</td>
<td>1.8</td>
<td>2.4/1.4</td>
<td>2.5</td>
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<td>Sampling (MHz)</td>
<td>256</td>
<td>312</td>
<td>76.8</td>
<td>245.76</td>
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<td>Feedback DAC</td>
<td>SCRZ</td>
<td>SCSR</td>
<td>SCR</td>
<td>CT-SI</td>
<td>CT-SC</td>
</tr>
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Conclusions

- Conventional feedback DACs have problems
  - NRZ DAC: Rise-fall asymmetry
  - RZ DAC: Jitter sensitivity
  - SC DAC: Poor linearity

- The SC-RZ DAC
  - Good marriage of the SC and RZ DACs

- A high performance CTDSM incorporating an SC-RZ DAC
  - 87 dB DR in a 2MHz bandwidth
  - 16.6mW in a 180nm CMOS process