Electronics and Energy Applications of 1D and 2D Nanomaterials

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  – Z. Bao, K. Goodson, S. Mitra, Y. Nishi, E. Reed, K. Saraswat, H.-S.P. Wong (Stanford), D. Cahill, W. King,
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What Motivates Us

20 Watts

200 kiloWatts

(conventional Moore’s Law size scaling can get us ~10x)

Electronics Use (and Waste) Much Power

Limited by power & heat since 2005!

energy limits performance from processors, to mobile devices, to data centers

MTF ~ \exp \left( \frac{E_A}{k_B T} \right)
Electronics Use (and Waste) Much Power

Calibrating: 1 GW ~ 1 nuclear power plant
12 GW ~ all electricity used by Argentina

Our Work: Two Sides of the Same Coin

Lower power at its source
(devices, sensors, circuits)

Harvest and manage heat
(energy, thermoelectrics)

fundamental understanding
practical applications
Outline of Talk

- **The SystemX Alliance at Stanford**
  - Center for Integrated Systems (CIS) → SystemX Alliance
    - Industry-academic Alliance to repositioned for 21st century research
    - Become "the" hub for electronic research at Stanford
  - What’s New?
    - Stronger emphasis of top-down, *systems research*
    - Introduce *focus areas* to create coherent thrusts
    - Additional *sponsor benefits* including workshops, E-Seminars

- **Transistors**
  - Heterogeneous integration of beyond-Si materials

- **Data Storage**
  - Approaching limits of phase-change memory

- **Thermal Energy at Nanoscale**
  - Ballistic heat flow and fundamental limits
### Value Proposition for Industry Sponsors

- **See everything** that is going on at Stanford
  - Real-time view of all faculty research, including NSF, DARPA, etc. activities
  - Student recruiting, internships, and networking
- **Participation in Focus Area research**
  - Invitation-only attendance to bi-annual workshop & discussion
- **Customized Fellow-Mentor-Advisor (FMA) projects**
  - Company-specific research performed by student & advisor with industry mentor
- **Faculty liaisons, company visits, and weekly E-Seminars**

### SystemX Focus Areas

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<th>Design Productivity</th>
<th>Energy/Power Management Systems</th>
<th>Internet of Everything</th>
<th>Bio Interfaces</th>
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- Focus areas change dynamically and have finite life-cycle (~3-5 years)
Heterogeneous Integration Focus Area

- Heterogeneous Integration of Everything onto Anything (HIEA)
- Integration of “beyond-Si” platforms for “beyond Moore” applications
  - Monolithic integration of logic, memory, sensors, thermal management, flexible substrates
  - Energy-efficient and brain-inspired design opportunities
  - Autonomous electronics and energy-harvesting opportunities


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  - Integration of electronics based on 2D materials
- Data Storage
  - Approaching limits of phase-change memory
- Thermal Energy at Nanoscale
  - Ballistic heat flow and fundamental limits
Transistors Beyond Silicon?

**Problem:** 20th century transistors “carved” out of 3D materials (Si) → surface roughness restricts mobility, band gap, variability

**Solution?** 21st century atomically thin materials

- 1D carbon nanotube (CNT)
- 2D TMD (MoS$_2$, WTe$_2$, ZrSe$_2$)
**Beyond-Silicon 2D Materials**

CVD growth of graphene, BN and MoS$_2$

- **BN**
- **monolayer MoS$_2$**
- **ZrSe$_2$**
- **HfSe$_2$**
- **WTe$_2$ (metallic)**

**CVT growth of MoTe$_2$, WTe$_2$, ZrSe$_2$, HfSe$_2$**

collab. H.S.-P. Wong, Y. Nishi, I. Fisher

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**Heterogeneous Integration Progress**

**Monolithic 3D:** low-temperature 3D integration of CNT logic and RRAM memory on CMOS substrate

- **CNFET**
- **RRAM**
- **Silicon**

**Wet or Dry Transfer:** layer transfer of 2D monolayers onto insulators while preserving the electronic properties

- **Cu-assisted Dry Transfer**
- **PMMA-assisted Wet Transfer**

source: Shulaker, Wong, Mitra (IEDM-2014)

source: K. Smilhe (Pop Lab, 2015)
Band Gaps ($E_G$) of Several 2D Materials

courtesy of M. Mleczko (Pop Lab)

High-Speed / RF

- Low-$E_G$ but high mobility $\rightarrow$ high-speed and RF applications
- Medium-$E_G$ (0.3 to 1.1 eV) $\rightarrow$ low-power CMOS
- High-$E_G$ $\rightarrow$ power devices

Low-Power CMOS
$\sim$0.5-1.2 eV

Graphene
0.67 eV
Ge
Si
1.11 eV
GaAs
1.42 eV

Black Phosphorus
0.3 eV (Bulk)
1.1 – 1.9 eV (1L)

Power Devices

- WSe$_2$, WS$_2$, MoS$_2$
  $-1.4 – 1.8$ eV 1L

Layered Insulators

h-BN

Early Work: Graphene Transport Parameters


Lack of transport data* at $T > 300$ K and high-field $v_{sat}$ (>1 V/μm)

High-field $v_{sat}$ measurement is tricky, needs constant field

Also extracted practical electrical and thermal compact models

Graphene Mobility – Where Does it Stand?

mobility = characterizes “ease” of current flow in a material; e.g. $I \propto \eta \mu E$

Today: Graphene-Based Functions and Systems

- Goal: graphene switched analog circuit (SAC). Why?
- Graphene = nanofabrics with high mobility (~10x > Si), flexible…
- SAC tolerates low $I_{on}/I_{off}$ ratio (~5x) of graphene (no band gap)
- Breakthroughs in heterogeneous integration of graphene & CMOS
Graphene Dot Product (GDOT) Nanofunction

- Dot product nanofunction used for image processing, neural networks...
- Takes advantage of native graphene properties, tolerates drawbacks

Idea:

Simulation:

weights encoded by pulse widths $\rho T$

Test Structures

- RF
- TLM
- MOScaps
- MIMcap

... and Implementation
CVD Growth of Monolayer MoS$_2$

Kirby Smithe (Pop Lab)

2” Tube Furnace Schematic

- S source
- Substrate + PTAS
- Mo$_3$
- Ar flow

PTAS: perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt

P = 760 Torr
T = 850 °C

90 nm SiO$_2$/Si (p++)

Continuous, mostly 1L MoS$_2$


Digital Electronics → Monolayer CVD MoS$_2$


- Large-area monolayer CVD MoS$_2$, direct band gap ~1.8 eV
- Wish to scale up devices for low-power digital electronics

Good current achieved (~275 µA/µm) in 80 nm device, but contact resistance remains dominant
**Scaled Semiconducting MoS₂ Transistors**

**Goal:** Aggressively scale 2D transistors (e.g. MoS₂) for ultra-low power digital electronics

- Demonstrated how **contacts are limiting** the performance of small MoS₂ transistors
- Built devices with ~40 nm channel length and variable contact sizing ($L_C = 20$ to 100 nm)
- **Smallest MoS₂ transistor with smallest contacts to date** (contacted gate pitch CGP ~ 70 nm, smaller than “22 nm” Si technology from Intel and Samsung)

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**Metal Contacts to MoS₂ (Clean but Undoped)**


- Contacting 2D materials is **difficult**
- Cleaner Au deposition (~$10^{-9}$ torr) leads to improved contact resistance
  - $R_C \approx 740 \, \Omega \cdot \mu m$ and $\rho_c = 4 \times 10^{-7} \, \Omega \cdot \text{cm}^2$

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2D Contacts to 2D Transistors

- WTe₂ (2D metal) contacts to WSe₂ (semic.)
- Residue-free transfer process
- 2x improvement over Ag contacts ("best known")
- Observed current saturation


Summary of Challenges in 2D Devices

Material Quality:

Contact Resistance (R_c):

Interfaces:

+Variability!

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Phase-Change Memory (PCM) Materials

- Chalcogenide compound: Ge$_2$Sb$_2$Te$_5$ (GST)
- Used in RW-DVDs
- Crystalline vs. amorphous: fast phase change (~1 ns)
- Large change in resistance (>100x)
- Promising candidate for memory, BUT... high programming current (~0.1 mA at IBM, Intel, Samsung)

References:
- Chen and Pop IEEE-TED (2009)
Phase-Change Memory with CNT Electrodes

- Key idea: CNTs are smallest possible electrodes (1-2 nm diameter)
- Use CNT to contact sub-10 nm bits of phase-change material
- Switching at ~100x lower power than conventional PCM!


Self-Aligned Nanotube-Nanowire Devices

- "Marshmallow" memory bit optimized for thermal confinement
- PCM nanowire self-aligned with CNT electrodes
- Excellent \( R_{\text{OFF}} / R_{\text{ON}} \) ratio (> 1000) approaches intrinsic GST limits

We Can Also Use Graphene Electrodes

- Graphene “edge” electrode enables sub-10 µA $I_{\text{reset}}$
- Heterogeneous integration challenges

Where These Results Fit In

- These devices are highly scalable with electrode and bit size
- Lowest power <1 µW, energy <1 fJ/bit (with ~1 ns pulse)
- Have not hit fundamental limits yet (~10-100x lower… 1.2 aJ/nm³)∗

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2D Material Thermal Properties

- **Large in-plane** thermal conductivity of graphene, BN (>500 W/m/K)
- **Ultra-low cross-plane** thermal conductivity of layered WSe₂ (<0.1 W/m/K)
  - Lower than plastics and comparable to air
- Huge thermal anisotropy in all layered 2D materials (>10-100x)
- MRS Bulletin review with AFRL:
  

- **Large thermopower** in TMDs (S ~ 0.5 mV/K) → Thermoelectrics?

\[ ZT = \frac{S^2 \sigma T}{k} \]
### Thermal Conductivity ($\kappa$) of 2D Materials

- Flexural phonon modes play important role in 2D materials
- **Anisotropy**: $\kappa_\parallel$ from $\sim6$ Wm$^{-1}$K$^{-1}$ (WTe$_2$) to $\sim2000$ Wm$^{-1}$K$^{-1}$ (graphene)
  - Cross-plane $\kappa_\perp$ is typically very small, e.g. $1$ to $6$ Wm$^{-1}$K$^{-1}$

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### Heat (and Current) Flow in Nanoscale Samples

- Macroscale, $R$ is additive: $1 + 1 = 2$
- **Nanoscale**, $R$ is quantized: $1 + 1 = 1$
  - Occurs when system size is comparable to electron or phonon (heat) wavelengths and mean free path (10-100 nm)
  - Both electrical and thermal resistance can be **quasi-ballistic**
Heat Flow in Nanoscale Graphene


Bulk thermal properties do not apply at <1 µm!
Thermal conductivity $k(T) = f(W,L)$ even at room $T$
- ~35% (quasi-)ballistic heat flow in short devices ($\lambda \sim 100$ nm)
- Strong edge scattering in narrow devices

Looking Ahead: Future Opportunities

collab: E. Reed, K. Goodson, K. Saraswat, H.-S.P. Wong, Y. Cui

Could we:
- Exploit anisotropy for routing heat? (thermal diode)
- Separate thermal and electrical flow? (thermal transistor)
- Design electronics with built-in thermoelectric cooling?
- Achieve transparent heat spreaders and flexible thermoelectrics?
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Summary

- Moore’s Law ~10x \(\rightarrow\) slowing down
- Energy scaling & harvesting ~10^4x \(\rightarrow\) exciting

- Opportunity for convergence of:
  - Novel nanomaterials
  - Low power devices
  - Anisotropy, ballistic, thermoelectric

- Understand fundamental limits
- Future opportunities

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