Blocker Tolerant Software Defined Receivers

Hooman Darabi

7/25/13
Receiver Noise and Linearity

• Receiver NF sets the sensitivity, range:

\[ \text{Sensitivity} = -174 + NF + 10\log(BW) + SNR \]

\[ 10\log(KT), \text{ dBm/Hz} \]

Set by the standard

• Small signal linearity:
  - \( IIP_2, IIP_3 \)

• Large signal linearity:
  - Gain compression

• Reciprocal mixing

• Harmonic mixing

Blockers: In/Out-Band

\[ 2f_{B1}-f_{B2} \quad f_{B1} \quad f_{B2} \]

\[ G \quad G_D \]

Operates here

\[ A_D \quad A_B \]
Reciprocal Mixing

- \( P_B + PN(\Delta_B) + 10 \times \text{LOG}(BW) = P_D - \text{SNR} \)
- \( \text{BNF} = 174 + PB + PN \)
Harmonic Rejection & Aliasing in Mixers

Square-wave LO harmonically rich
More phases alleviates the issue
More energy in main, less in higher harmonics

\[ \text{Aliasing} = 1 + \frac{1}{3^2} + \frac{1}{5^2} + \ldots = \frac{\pi^2}{2} \]

\[ \frac{M}{\pi} \sin \left( \frac{\pi}{M} \right) \]

\[ M = 2, 4, 8, 16, 32 \]

Weldon, JSSC 2001
3/4G Full-Duplex Problem

- Duplexer is a dual-band filter
- Similar issue due to co-existence
Ideal Receiver

- Filter only rejects out-of-band blockers
- In-band blockers require a high-resolution ADC
- Power hungry

- Invented by Armstrong in 1918
- *Down-conversion* reduces the ADC resolution
- Lower power
Ideal Receiver – Challenges

- Scalable
- Broad-band: Low-noise, Blocker tolerant
- Low-power
Narrow-Band Filtering Concerns

- Large blockers compress the receiver
- External filtering is narrow-band and costly

Multi-Band Receiver

Switch

15-20dB

0dBm

-99dBm

6.6V p-p
N-Path Filtering Concept

- Very high-Q passives needed
- *N-path filtering* extends Nyquist rate

\[ NY = N \times \left( \frac{f_c}{2} \right) \]

\[ f_c \quad 2f_c \]

---

\[ L. \text{ Franks, Bell Syst. Tech. J., 1960} \]
Passive Mixers as High-Q Filters

\[ Z_{in}(s) \approx R_{SW} + \frac{2}{\pi^2} \{Z_{BB}(s - j\omega_{LO}) + Z_{BB}(s + j\omega_{LO}) \} \]

High-Q BPF from low-Q LPF

Mirzaei, TCAS 2010
Current-Mode Receivers

- Passive mixers to achieve high-Q filtering
- Current mode LNA: LNTA
- Enhance the blocker tolerance
Front-End Matching Concerns

- Wide-band matching
- Good linearity
- NF suffers

\[ R_s = 50 \Omega \]

\[ \text{NF} > 3 \text{dB} \]

- Narrow-band matching
- Good NF
- Modest linearity
Mixer-First Receivers

• For M phases:  \[ F = \left[ 1 + \frac{r_{DS}(ON)}{R_s} + \frac{V_{bb}^2}{M (4KTR_s)} \right] \times N_{\text{Aliasing}} \]

• \[ N = \frac{1}{(\text{sinc} (\pi/M))^2} > 1 \]

• NF > 3dB in practice at GHz frequencies

Andrews, JSSC 2010
Noise Cancelling Concept

- Used in broad-band LNA’s
- Poor linearity

\[ r_m = \alpha \times R_s \]

\[ R_{IN} = R_S \]

\[ V_{IN} \]

\[ V_{OUT} \]

\[ I_{IN} \]

\[ \alpha \]

\[ V_{IN} \]

\[ r_m I_{IN} \]

\[ -r_m I_{IN} \]

\[ N_F \]

\[ R_{Relative Gain} \]

Bruccoleri, ISSCC 2002
Noise Cancelling RX Architecture

- Low noise and linear
- No Balun required

\[
R_S = R_{SW} + \frac{2R_{BB}}{\pi^2}
\]

\[
\alpha = -G_M \times R_{LA}
\]

\[
BW << \Delta f_B
\]

\[
r_m = R_{LM}
\]

\[Murphy, ISSCC 2012\]
**Noise & Linearity Performance of NC RX**

- $G_M$ noise dominant, no need to provide matching:
  \[ F \approx (1+\frac{v_{GM}^2}{4KTR_S}) \times N \]

- Similarly main path distortion cancelled:
  \[ IIP_3 \approx (1+\frac{R_S}{R_{IN}})^{3/2} \times IIP_{3\_AUX} \]
Over-Sampling Mixer Architecture

- Synthesizes arbitrary 8-phase LO: \( V_{OUT} = i_{RF}(t) \sum_{x=0}^{7} K_x s(t - \frac{x}{8T}) \)
Complete NC Receiver Architecture

\[
NF \approx 1 + 1/G_M R_S
\]

\[
10\Omega
\]

\[
50\Omega
\]
RF $G_M$ Cell

- Class AB transconductance
- Scalable
- Linear due to class AB and low-impedance loading

Approximately $10\,\Omega$
Baseband TIA

- Most power efficient
- Noise: $v_{bb}^2 \approx 4KT\gamma/G_m \approx 4KT/40I_D$
- Input resistance: $R_{in} \approx R_F / A_{OPEN} \approx R_F / (G_m(R_F||R_L))$
Receiver Scalability

2-Phase

\[ V_{DD} \]

\[ t_r \]

\[ t_f \]

\[ T = 8t_r \]

\[ S \times T = 8V_{DD} \]

8-Phase

\[ V_{DD} \]

\[ 4t_r \]

\[ T = 32t_r \]

\[ S \times T = 8V_{DD} \]

• Inherently relies on high-speed logic, switches

• In 40nm, \( t_r \approx 10pS \):
  – 12.5GHz for 2-phase (overlapping)
  – 3.12GHz for 8-phase

• Scales w/ technology
Noise Figure

• 1/f corner reduces from 100kHz to less than 10kHz

• Corresponds to <-113dBm GSM sensitivity
• 4.1dB 0dBm BNF, mostly limited by reciprocal mixing
Linearity

- Close to 0dBm 1dB compression at maximum gain
NF vs. Relative Phase Correction

- Robust at optimum point

 NF, dB

Relative Phase, °

Uncompensated
## Summary of Performance

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Mixer first</th>
<th>NC LNA</th>
<th>NB SAW-Less</th>
<th>NC RX</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Range</td>
<td>0.1-2.4GHz</td>
<td>0.4-6GHz</td>
<td>900/1800</td>
<td>0.1-2.7GHz</td>
</tr>
<tr>
<td>Input</td>
<td>SE</td>
<td>Differential</td>
<td>Differential</td>
<td>SE</td>
</tr>
<tr>
<td>NF at 2GHz</td>
<td>7dB</td>
<td>4.4dB</td>
<td>4.1dB</td>
<td>1.8dB</td>
</tr>
<tr>
<td>0dBm BNF</td>
<td>NA</td>
<td>13dB</td>
<td>7dB</td>
<td>4.1dB</td>
</tr>
<tr>
<td>3rd/5th HR</td>
<td>35/43dB</td>
<td>None</td>
<td>None</td>
<td>42/45dB</td>
</tr>
<tr>
<td>OB IIP3</td>
<td>25dBm</td>
<td>10dBm</td>
<td>NA</td>
<td>14dBm</td>
</tr>
<tr>
<td>RX Current</td>
<td>12mA</td>
<td>12mA</td>
<td>37mA</td>
<td>12mA</td>
</tr>
<tr>
<td>Area</td>
<td>2mm²</td>
<td>2mm²</td>
<td>1.4mm²</td>
<td>1.2mm²</td>
</tr>
<tr>
<td>Technology</td>
<td>65nm</td>
<td>40nm</td>
<td>65nm</td>
<td>40nm</td>
</tr>
</tbody>
</table>
**NC RX Die Photo**

- **Die area:** 1.2mm²
- **Inductor-less**
Reciprocal Mixing Issue – System Approach

Reciprocal mixing $NF = 174 - P_B - PN$

- Start w/ a low-power/cost VCO
- Deal with its consequences in system level
- Proper phase noise estimation is key
Symmetry of Reciprocal Mixing

Phase noise at $+\Delta f_b$ and $-\Delta f_b$ are correlated

Reciprocal mixing

Desired signal
RM Cancellation Architecture

Wideband PLL
(Low Frequency & Low Power, >20dB spec relaxation)
Limiter Based Architecture
Noise Aliasing in a Limiter

Harmonic Recombination

Limiter1

Limiter2

Limiter3

Limiter4
Protoype RM Cancelling Receiver
• Blocker offset as low as 10MHz
• SS NF of about 2.4dB
RM Cancelling RX Die Photo

- 40nm CMOS, 1.4mm²
Receiver Architecture for Coexistence

- Second path to divert blocker away
- Relaxes noise and linearity of main receiver

Reciprocal mixing $\text{NF} = 174 - P_B - \text{PN}$
N-Path Impedance Implementation

- Clocker by the aggressor TX LO

25% duty-cycle clocks @ $f_b$

$f_{-3dB,h} (f_{-3dB,h} \ll f_b)$

TX Signal
Coexistence Receiver Architecture

- LC-match
- \( G_m \)
- \( P_{RX} \)
- \( P_b \)
- \( f_b \)
- \( f_{RX} \)

\[ H_1(f) \]

Main path TF

\[ H_2(f) \]

Aux path TF

\( f_b \) \quad \( f_{RX} \)
Measured Blocker Noise Figure

- \( \text{NF} > 25\text{dB} \) if Aux path de-activated

Desired at 2GHz, Blocker at 1.9GHz

- \( \text{NF} > 25\text{dB} \) if Aux path de-activated
### RX Performance Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF, dB</td>
<td>2.5</td>
<td>2.5</td>
<td>4</td>
<td>1.7</td>
</tr>
<tr>
<td>OB IIP3, dBm</td>
<td>-2.5</td>
<td>-4</td>
<td>-14</td>
<td>-2.5</td>
</tr>
<tr>
<td>OB IIP2, dBm</td>
<td>&gt; 50</td>
<td>58</td>
<td>N/A</td>
<td>&gt; 50</td>
</tr>
<tr>
<td>0dBm Blocker NF, dB</td>
<td>N/A</td>
<td></td>
<td></td>
<td>13.5</td>
</tr>
<tr>
<td>Battery Current, mA</td>
<td>65</td>
<td>44</td>
<td>46</td>
<td>10</td>
</tr>
<tr>
<td>Total RX Area, mm²</td>
<td>6.7</td>
<td>3.4</td>
<td>2.2</td>
<td>0.93</td>
</tr>
<tr>
<td>Technology</td>
<td>130nm</td>
<td>90nm</td>
<td>65nm</td>
<td>40nm</td>
</tr>
<tr>
<td>Application</td>
<td>Cellular</td>
<td>Cellular</td>
<td>WiFi</td>
<td>Generic</td>
</tr>
</tbody>
</table>

Coexistence RX Die Photo

40nm CMOS with active area of 0.93mm²
Summary & Conclusions

- Scalable
- Immune to large blockers and/or low-power