Silicon and wireless will continue changing our daily lifestyle. Modern CMOS technology with transistor $f_T$ and $f_{MAX}$ exceeding 300 GHz has opened the door for a very fertile research and new product area that demands innovation to meet challenges in all levels, from device, circuits, architecture, system and on-chip-antenna. The newly released IEEE 802.11ad triple-band (2.4/5/60-GHz) WLAN standard supports data transmission rates up to 7 Gbps. This short course is targeted at both beginners and advanced RF/Analog IC designers. It will include system considerations, device modeling and IC design. The course will cover but is not limited to the following:

- Overview of Nanoscaled CMOS technology
- How to Designs Gbps Radio Component Circuits
  - Transceiver
  - Amplifier
  - (de)modulator
  - high-speed ADC/DAC
  - Architectures and Power Estimates
  - Scalable Device Modeling
  - On-chip antenna design

**About the Instructors:**

**Dr. Frank Chang** is the Wintek Chair Professor in the Electrical Engineering Department, and the Director of the High Speed Electronics Laboratory, at the University of California, Los Angeles (UCLA).

Before joining UCLA, he was the Assistant Director and Department Manager of the High Speed Electronics Laboratory at the Rockwell Science Center (1983-1997), Thousand Oaks, California. In this tenure, he successfully developed and transferred AlGaAs/GaAs Heterojunction Bipolar Transistor (HBT) and BiFET (Planar HBT/MESFET) integrated circuits technologies form the research laboratory to the production line (now Conexant Systems and Skyworks). The HBT and BiFET productions have grown into multi-billion dollar businesses worldwide. Throughout his career, his research has been mostly in the development of high-speed semiconductor devices and integrated circuits for RF & mixed-signal communication and sensing system applications. He was the principal investigator at Rockwell to lead the US DARPA ADC and DAC development for direct conversion transceiver (DCT) and digital radar receivers (DRR) systems. He was the inventor of the multi-band, re-configurable RF-Interconnects based on FDMA and CDMA multiple access algorithms for intra- and inter-ULSI communications. He pioneered the development of world’s first multi-gigabit/sec ADC, DAC and DDS in both GaAs HBT and Si CMOS technologies and the first 60GHz radio transceiver based on transformer-folded-cascode (Origami) circuit architecture and low phase noise VCO with embedded digitally controlled artificial dielectric (DiCAD). He was also the first to demonstrate CMOS RFICs in the Tera-Hertz frequency range of 1.3THz. Dr. Chang has authored or co-authored over 280 technical papers, 10 book chapters, authored 1 book, edited 1 book and holds 20 U.S. patents. He was an editor of the IEEE Transactions on Electron Devices (1999-2001) and served as a guest editor for the IEEE Journal of Solid-State Circuits in 1991 and 1992 and for the Journal of High-Speed Electronics and Systems in 1994.

Dr. Chang was elected to the National Academy of Engineering in 2008, for the development and commercialization of GaAs power amplifiers and integrated circuits. He received the IEEE David Sarnoff Award in 2006 and became a Fellow of IEEE in 1996. He also received Rockwell's Leonardo Da Vinci Award (Engineer of the Year) in 1992, National Chiao Tung University's Distinguished Alumnus Award in 1997 and National Tsing Hua University's Distinguished Alumnus Award in 2002.
Fujiang Lin (M’93–SM’99) received the B.S. and M.S. degrees from the University of Science and Technology of China (USTC), Hefei, China, in 1982 and 1984, respectively, and the Dr.-Ing. degree from the University of Kassel, Kassel, Germany, in 1993, all in electrical engineering. In 1995, he joined the Institute of Microelectronics (IME), Singapore, as a Member of Technical Staff, where he pioneered practical RF modeling for MMIC/RFIC development. In 1999, he joined HP EEs of, as the Technical Director, where he established the Singapore Microelectronics Modeling Center, providing accurate state-of-the-art device and package characterization and modeling solution service worldwide. From 2001 to 2002, he started up and headed Transilica Singapore Pte., Ltd., a research and development design center of Transilica Inc., a Bluetooth and IEEE 802.11 a/b wireless system-on-chip (SoC) company. The company was acquired by Microtune Inc. After the close down of Transilica Singapore in 2002, he joined Chartered Semiconductor Manufacturing Ltd., (third largest foundry), as Director, where he led the SPICE modeling team in support of company business. In 2003, he rejoined IME as a Senior Member of Technical Staff, where he is currently focused on upstream research and development initiatives and leadership towards next waves. His current research interest is in the development of CMOS as a cost-effective technology platform for 60-GHz band millimeter-wave SoC. As an Adjunct Associate Professor with the National University of Singapore, Singapore, and Adjunct Professor with USTC, Hefei, China, he is actively involved in educating and training post-graduate students. He has authored or coauthored over 100 scientific papers. He holds five patents. Dr. Lin has served IEEE activities in different functions since 1995 including chair of the IEEE Singapore MTT/AP Chapter, committee member of Singapore Section, reviewer board member for a few of Transactions or Journals, and Technical Program Committee (TPC) member of numerous conferences such as RFIC and ESSCIRC. He is initiator and co-organizer of international workshops and short courses at APMC99, SPIE00, ISAP06, and IMS07. Recently, he and his team initiated and organized the IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Singapore.

Dr. Lin was the recipient of the 1998 Innovator Award presented by EDN Asia Magazine. Most recently, he has been selected by the Chinese National “Thousand Talents Program”. He will back USTC in Hefei, China to lead their research and education in Electronic Science and Technology.

Benefits of this Course

- To learn directly from a world distinguished lecturer
- System driven considerations
- Building blocks challenges
- Device/process integration

Who Should Attend?

Engineers and technical staff, managers and business development personnel, students, who are keen on learning about RF and analog IC design in CMOS.

Date: Tuesday, 19 October 2010, Time: 0830 – 1730 (Registration starts at 8:30am, Lecturer starts at 9:00)

Venue: Lecture Theater 24, South Spine, Nanyang Technological University
50 Nanyang Avenue, Singapore 639798 (see attached map)

Fees:
- $500 for regular participant
- $300 for IEEE Member by providing Membership No.
- (discount for group registration from the same company: pay two get additional one free, pay five get additional three free)
- $75 for regular students and
- $50 for IEEE student members by providing Membership No.

(Hardcopy of lecture notes, Lunch and refreshments will be provided)
Registration Deadline: 12th October 2010

Registration Form

(IEEE Member #)

Name: ____________________________ Email: ____________________________
Name: ____________________________ Email: ____________________________
Name: ____________________________ Email: ____________________________

Company: ____________________________
Address: ____________________________
Tel: __________________ Fax: ____________________________

Email of contact person for group registration: ____________________________

An invoice will be issued to your company upon successful registration.
Email to: atenga.mary@gmail.com, Short Course Administrator,
Tel: +65 9030 9898 or Fax to: +65 68413986
Please email all technical enquiries to Fujiang_Lin@ieee.org,
Location of LT24 at SOUTH SPINE level B2, NTU Jurong Campus